

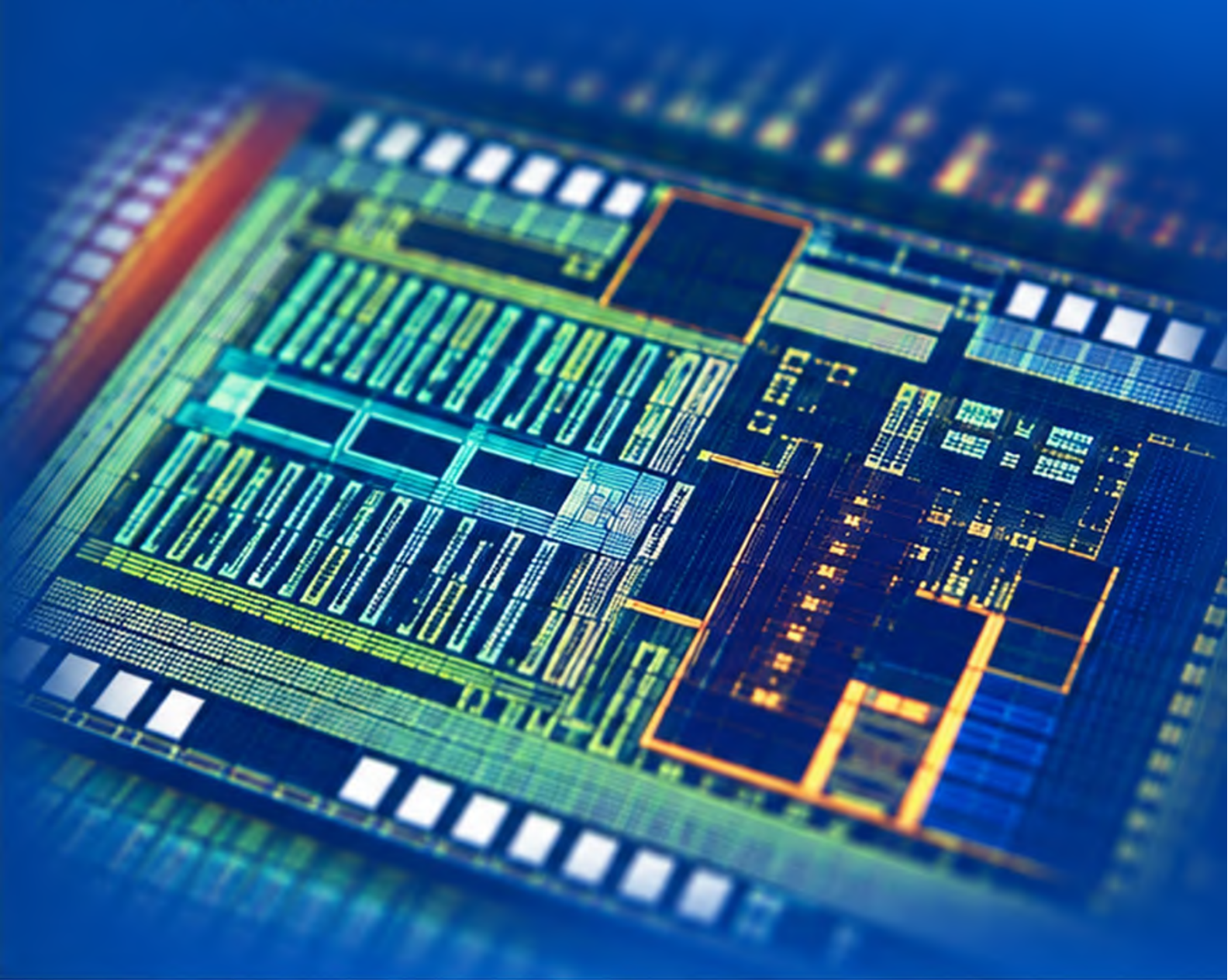
INSA-DFG-IIT Madras

Indo-German

Early-Career Scientist Workshop
on Chip Design

5-7. October 2026

Chennai, India



INSA

Indian National
Science Academy



Deutsche
Forschungsgemeinschaft
German Research Foundation



IIT Madras

Indian Institute
of Technology Madras

Early-Career Scientist Workshop on Chip Design

Dear colleagues from India and Germany,

We are delighted to welcome you to the INSA-DFG-IIT Madras Indo-German Early-Career Scientist Workshop on Chip Design in Chennai! This initiative is organized by the Indian National Science Academy (INSA) and the German Research Foundation (Deutsche Forschungsgemeinschaft, DFG). Serving as the scientific conveners are Prof. Shanti Pavan (Indian Institute of Technology, Madras) and Prof. Holger Blume (Leibniz University Hannover).

The primary goal of this meeting is to foster strong networks among researchers who will shape the future of scientific cooperation between India and Germany.

Over the next three days, we hope to spark vibrant interactions, fruitful discussions, and meaningful exchanges regarding future collaborations.

We wish you an inspiring workshop and many successful partnerships ahead.

Organizing Committee of the Early-Career Scientist Workshop on Chip Design

Message from the President, INSA

It gives me immense pleasure to welcome all participants to the **INSA–DFG–IIT Madras Workshop on Chip Design**, being organized by the **Indian National Science Academy (INSA)** in collaboration with the **German Research Foundation (DFG)** and with the academic support of the **Indian Institute of Technology Madras (IIT Madras)**.

Semiconductor technologies and chip design are at the heart of modern digital transformation and are increasingly important for technological self-reliance, economic growth, and national security. Rapid advances in artificial intelligence, high-performance computing, communications, and emerging digital technologies have further underscored the need for sustained research and innovation in this strategically important field. In this context, strengthening international scientific partnerships and nurturing the next generation of researchers are particularly timely.

This workshop brings together early-career researchers and established experts from India and Germany to exchange ideas, share emerging research perspectives, and explore opportunities for meaningful and sustained collaboration in chip design. I am confident that the focused scientific discussions and interactions during the workshop will foster new research linkages, encourage collaborative initiatives, and contribute to building a strong Indo–German research ecosystem in semiconductor technologies.

I would like to acknowledge the valuable efforts of **Prof. Holger Blume**, Scientific Convener from Germany, and **Prof. Shanthi Pavan**, Scientific Convener from India, whose academic leadership has been instrumental in shaping this programme. I also appreciate the support of DFG, IIT Madras, and SRM Institute of Science and Technology in bringing this initiative to fruition.

I hope that the workshop will provide a stimulating platform for scientific exchange and lead to enduring partnerships among researchers and institutions in both countries.

I extend my best wishes to all the participants and organizers for a successful and productive workshop.

Prof. Shekhar C. Mande

President

Indian National Science Academy

Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026



Message from the Scientific Conveners

Chip design sits at an unusual point in the research landscape. It is an intensely practical discipline - the ideas either work in silicon or they do not - and at the same time it draws on device physics, circuit theory, signal processing, computer architecture and design automation. No single group, and increasingly no single country, spans all of it. Progress therefore depends heavily on the willingness of people working on different pieces of the problem to talk to one another.

That is the premise of this workshop. Over three days at SRM Institute of Science and Technology in Chennai, roughly two dozen early career researchers from Germany and India will present their work and, more importantly, argue about it. The topics deliberately span a wide range - data converters and RF front-ends, digital architectures and accelerators, hardware for machine learning, design methodology and verification. The programme is single-track, so everyone hears everything. Grouping such diverse work into neat sessions proved impossible; we decided this was a feature rather than a defect.

The participants are at a stage in their careers - late doctoral, postdoctoral, early faculty - when collaborations formed are likely to last for decades. India and Germany both have strong and complementary capabilities in microelectronics, and both are investing seriously in the area. What has been missing is sustained personal contact at the working level between the people who will actually build the next generation of chips.

Our goal for these three days is modest and specific: that each participant leaves with a clear picture of what the others are doing, and with at least one or two conversations worth continuing after everyone has flown home. If a handful of joint proposals, student exchanges or co-authored papers follow, the workshop will have done its job.

We are grateful to INSA and the DFG for making this possible, and to SRMIST for hosting us.





Freedom of research and an effective research system are indispensable prerequisites of an open society. The promotion of the sciences and humanities forms part of Germany's cultural and political identity and contributes significantly to prosperity and sustainable progress.

These are the guiding principles underlying the work of the

Deutsche Forschungsgemeinschaft (DFG, German Research Foundation).

The DFG is the largest research funding organisation and central self-governing organisation for the sciences and humanities in Germany. It serves the sciences and humanities in all their forms and disciplines and promotes research of the highest quality. All of its procedures are based on scientific criteria.

The DFG primarily funds knowledge-driven research projects developed by the researchers themselves, focuses on funding basic research and provides space for the pursuit of high-risk and unconventional research questions.

Jointly funded by the federal and the state governments the DFG takes on responsibility for the further advancement of the German and European research systems.

The DFG shapes structures and fosters cohesion. It assumes its strategic responsibility in commitment to the spirit of freedom of research and to ethical principles.

As a centre for research, promoting its adaptability, flexibility, inclusiveness and diversity, the DFG works to ensure the effectiveness and appeal of Germany.





The **Indian National Science Academy (INSA)** was established in 1935 and is India's premier scientific academy and an autonomous professional body under the Department of Science and Technology (DST), Government of India. Its mandate is to promote science in India, identify and nurture scientific talent, and leverage scientific knowledge for the advancement of humanity and the welfare of the nation. For more than nine decades, INSA has served as an en-

abler, think tank, and mentor for Indian science, with a strong commitment to serving society.

INSA draws upon the collective knowledge and expertise of its more than 1100 Fellows, representing diverse branches of science, including physical, chemical, biological, agricultural, medical, and interdisciplinary sciences, as well as the history of science. The Academy also recognizes and promotes outstanding contributions towards the translation of scientific knowledge for societal benefit.

INSA organizes and supports seminars, conferences, workshops, training programmes, lectures, and other scientific activities addressing issues of national and societal significance and leveraging the expertise of its Fellows. Through its inter-academy activities, INSA also conducts refresher courses and training programmes for teachers and contributes to the dissemination of scientific knowledge through reports, policy papers, books, journals, and other publications.

INSA has been a member of the International Science Council (ISC) and its predecessor organizations since 1968, representing Indian science in international scientific forums. The Academy also maintains MoUs and bilateral agreements with national academies and scientific organizations in several countries to promote international scientific cooperation and facilitate the exchange of knowledge and expertise.

INSA represents Indian science on major international platforms and in global scientific networks, including Science20 (S20), BRICS Science Academies Forum, InterAcademy Partnership (IAP), Science Council of Asia (SCAR), Association of Academies and Societies of Sciences in Asia (AASSA), and other international bodies and initiatives, as appropriate.

For more information, please visit the INSA website: www.insaindia.res.in



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026



PROGRAMME

Early-Career Scientist Workshop on Chip Design, October 5 – 7, 2026		
Venue: Dr. Ramanujam Hall, TP107, SRM Institute of Science and Technology, Chennai		
Day 0, Sunday, October 4, 2026		
Arrival of the participants @Chennai Airport		
Pick up from the airport according to the flight details (coordination through INSA and SRM Hotel)		
13:00 – 19:00	Potential cultural visit to Mahabalipuram	
19:30 – 21:00	Kick-off Networking Dinner	Restaurant SRM Hotel
Day 1, Monday, October 5, 2026		
Time	Title	Speakers
09:00 – 09:30	Welcome Addresses INSA, DFG, IIT Madras, SRM University	
09:30 – 10:00	Session 1: Design of Application Specific Processors – From Medical Implants to Industrial Applications	Prof. Dr. Holger Blume Leibniz University Hanover
10:00 – 10:30	Session 2 Wideband Filtering Analog-to-Digital Converters using Continuous-Time Pipelining	Prof. Dr. Shanthi Pavan Indian Institute of Technology (IIT), Madras
10:30 – 11:00	Coffee Break	
11:00 – 11:30	Session 3: HOT-RISC-V: Architecture–Technology Co-Design for High-Performance Computing at 200 °C	Dr. Malte Hawich Leibniz University Hanover
11:30 – 12:00	Session 4: Brain Computer Interface for Neuromodulation System on Chips	Dr. Laxmeesha Somappa Indian Institute Technology (IIT), Bombay
12:00 – 12:30	Coffee Break	



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

12:30 – 13:00	Session 5: Tailoring Adaptive Voltage Scaling to the Constraints of FPGAs	Dr. Christoph Niemann University of Rostock
13:00 – 13:30	Session 6: Higher-Order N-Path Filters for Next-Generation Wireless Front Ends	Dr. Sashank Krishnamurthy Indian Institute of Technology (IIT), Madras
13:30 – 14:30	Lunch Break	
14:30 – 15:00	Session 7: Designing a Secure Compute-In-Memory Accelerator	Dr. Melvin Galicia RWTH Aachen University
15:00 – 15:30	Session 8: Demystifying Quantum Computing: A Circuit-Level Approach to Silicon Spin Qubits	Dr. Saravana Kumar Manivanan Indian Institute of Technology (IIT), Roorkee
15:30 – 16:00	Coffee Break	
16:00 – 16:30	Session 9: Integrated Circuit Research at the Institute for CMOS Design: Current Activities and Perspectives toward 140 GHz PMCW Radar	Dr. Justin Romstadt TU Braunschweig
16:30 – 17:00	Session 10: Complementary SiGe RF Front-End Circuits for FR3 and mm-Wave Applications	Dr. Prateek Sharma Indian Institute of Technology (IIT), Tirupati
17:00 – 17:30	Coffee Break	
17:30 – 18:00	Session 11: Shaping the future of wireless connectivity with transceiver and antenna chips co-design	Dr. Shahanawaz Kamal Barkhausen Institut
18:00 – 18:30	Session 12: From Advanced Semiconductor Devices to Energy-Efficient Integrated Circuits	Dr. M. Durga Prakash SRM University-AP
Dinner @ Restaurant SRM Hotel		



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Day 2, Tuesday, October 6, 2026		
Time	Title	Speakers
09:00 – 09:30	Session 13: Anyone Can Print a Biochip: From Manual Designs to 3D-Printed Microfluidics	Dr. Yushen Zhang Technical University of Munich
09:30 – 10:00	Session 14: Automatic Analog/RF Layout Synthesis using Open-source Tools	Dr. Ramprasath S Indian Institute of Technology (IIT), Madras
10:00 – 10:30	Coffee Break	
10:30 – 11:00	Session 15: Microelectronic Design - It's all about Energy Efficiency	Dr. Prof. Norbert When RPTU University Kaiserslautern-Landau
11:00 – 11:30	Session 16: Designing Energy-Efficient Mixed-Signal and RF ICs for Next-Generation Computing and Communication Systems	Dr. J. Manjula SRM Institute of Science and Technology, Chennai
11:30 – 12:00	Coffee Break	
12:00 – 12:30	Session 17: Low-Power and Smart IoT Circuit and System Design	Dr. Pengcheng Xu Technical University of Munich
12:30 – 13:00	Session 18: Advances in Integrated GaN Power Modules: Challenges, Solutions, and Applications	Dr. Raveesh Magod Indian Institute of Technology (IIT), Madras
13:00 – 14:00	Lunch Break	
14:00 – 20:00	Visit to IIT-Madras Followed by a Networking Dinner	



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Day 3, Wednesday, October 7, 2026		
09:00 – 09:30	Session 19: Hardware for AI and AI for Hardware Design – From Edge Intelligence to Agentic Design Automation	Dr. Lukas Krupp RPTU Kaiserslautern-Landau
09:30 – 10:00	Session 20: Efficient Hardware Acceleration for Emerging Security Applications	Dr. Utsav Banerjee Indian Institute of Science (IISc), Bangalore
10:00 – 10:30	Coffee Break	
10:30 – 11:00	Session 21: Masur: A Collaborative Chip Design Platform	Dr. Mattis Hasler Barkhausen Institut
11:00 – 11:30	Session 22: Challenges of cmos image sensor design	Dr. Kapil Jainwal Indian Institute of Technology (IIT), Hyderabad
11:30 – 12:00	Coffee Break	
12:00 – 12:30	Session 23: Intelligence at the Edge: Designing AI Within the Energy Budget	Dr. Viveka Konandur Rajanna Indian Institute of Science (IISc), Bangalore
12:30 – 13:00	Session 24: CMOS Low-Noise Amplifier Design: Challenges, Trade-offs and Emerging Trends	Dr. Andrew Roobert SRM Institute of Science and Technology, Chennai
13:00 – 14:00	Lunch Break	
14:00 – 14:30	Session 25: Invent a Chip: Opening Microelectronics to Future Chip Designers	Dr. Nils Hendrik Stanislawski Leibniz University Hannover



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

14:30 – 15:00	Session 26: A Zero-Crossing-Based Time-Domain Receiver for Monostatic FMCW Radar	Dr. Abhishek Kumar Indian Institute of Technology (IIT), Hyderabad
15:00 – 15:30	Coffee Break	
15:30 – 16:00	Session 27: Karlsruhe Institute Hardware/Software Co-Design for Integrated AI Systems of Technology (KIT)	Dr. Tanja Harbaum Karlsruher Institute of Technology (KIT)
16:00 – 16:30	Session 28: Revisiting RF IQ Calibration: A Perturbation-Based Approach for Fast, Lean and Accurate IQ Calibration of RF Receivers	Dr. Rahul Singh Indian Institute of Technology (IIT), Bombay
16:30 – 17:30	Discussion about steps going forward Short presentation by DFG about funding options for Indo-German research collaborations	Dr. Ina Strauß /Dr. Franziska Langer DFG
For participants leaving on Wednesday, October 7 Check-out from the hotel and travel to the airport according to the flight details (coordination through INSA and SRM Hotel) For participants leaving during the night/next day 19.30 Dinner @ Restaurant SRM Hotel		



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Conveners:

Prof. Dr. Holger Blume

Professor for "Architectures and Systems",
Managing Director of the Institute for Microelectronic Systems (IMS), Leibniz University Hannover

Prof. Dr. Shanthi Pavan

Dean (Academic Research), NT Alexander
Institute Chair Professor in the Department
of Electrical Engineering and Chairperson
of the Curriculum Task Force, Indian Institute of Technology (IIT), Madras



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

List of Attendees (Alphabetically)

Utsav Banerjee	Indian Institute of Science (IISc), Bangalore, <i>Department of Electrical Engineering</i>
Holger Blume	Leibniz University of Hannover, Managing Director of the Institute for Microelectronic Systems (IMS)
Melvin Galicia	University of RWTH Aachen, Institute for Communication Technologies and Embedded Systems, <i>Postdoctoral Researcher</i>
Tanja Renate Harbaum	Karlsruher Institute of Technology (KIT), <i>Team leader of the working groups "Design of adaptive hardware architectures" and "AI in embedded systems"</i>
Mattis Michel Hasler	Barkhausen Institut, Scalable Computing Hardware, <i>Senior Researcher</i>
Malte Gerriet Hawich	Leibniz University of Hannover, Department of Microelectronic Systems, <i>Research Staff at the Architectures and Systems Group</i>
Manjula J	SRM Institute of Science and Technology, Department of Electronics & Communication, Faculty of Engineering & Technology, <i>Associate Professor</i>
Kapil Jainwal	Indian Institute of Technology (IIT), Hyderabad, Department of Electrical Engineering, <i>Assistant Professor</i>
Shahanawaz Shahed Kamal	Barkhausen Institut, Radio Frequency Design Enablement Group, <i>Senior Researcher</i>
Sashank Krishnamurthy	Indian Institute of Technology (IIT), Madras, Department of Electrical Engineering, <i>Assistant Professor</i>
Lukas Krupp	RPTU University Kaiserslautern-Landau, Department of Microelectronic Systems Design, <i>Postdoctoral Researcher</i>
Abhishek Kumar	Indian Institute of Technology (IIT), Hyderabad, Department of Electrical Engineering <i>Assistant Professor</i>
Raveesh Magod	Indian Institute of Technology (IIT), Madras, <i>Assistant Professor in the Department of Electrical Engineering</i>
Saravana Kumar Manivanan	Indian Institute of Technology (IIT), Roorkee, Department of Electronics and Communication Engineering, <i>Assistant Professor</i>



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Christoph Ulrich Niemann	University of Rostock, Institute of Applied Microelectronics and Computer Engineering, <i>Postdoctoral Researcher</i>
Shanthi Pavan	Indian Institute of Technology (IIT), Madras, Department of Electrical Engineering, <i>NT Alexander Institute Chair Professor</i>
M. Durga Prakash	SRM University- AP, Department of Electronics and Communication Engineering, <i>Associate Professor</i>
Viveka Konandur Rajanna	Indian Institute of Science (IISc), Bangalore, Department of Electronic Systems Engineering, <i>Assistant Professor</i>
S Ramprasath	Indian Institute of Technology (IIT), Madras, Department of Electrical Engineering, <i>Assistant Professor</i>
Justin Romstadt	TU Braunschweig, <i>Head of the RF Systems and Circuits working group</i>
A. Andrew Roobert	SRM Institute of Science and Technology, Kattankulathur, Department of Electronics and Communication Engineering, <i>Assistant Professor</i>
Prateek Kumar Sharma	Indian Institute of Technology (IIT), Tirupati, Department of Electrical Engineering, <i>Assistant Professor</i>
Rahul Singh	Indian Institute of Technology (IIT), Bombay, Department of Electrical Engineering, <i>Assistant Professor</i>
Laxmeesha Somappa	Indian Institute of Technology Bombay, Department of Electrical Engineering, <i>Assistant Professor</i>
Nils Hendrik Stanislawski	Leibniz University of Hannover, <i>Researcher at the Faculty of Electrical Engineering and Computer Science</i>
Norbert Hans Wehn	RPTU University Kaiserslautern-Landau, Department of Microelectronic Systems Design, <i>Professor of Electrical and Information Technology</i>
Pengcheng Xu	Technical University of Munich, Department of Electrical Engineering, <i>Senior Researcher</i>
Yushen Zhang	Technical University of Munich, Chair of Electronic Design Automation, <i>Research Fellow</i>



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Organizers

Vaibhav Agarwal
Franziska Langer
Ina Strauss

DFG Office India
DFG International Affairs, DFG Office India
DFG Scientific Affairs, Bonn

Debashis Mitra

INSA, International Division; ICMR Emeritus Scientist at BRIC-
National Centre for Cell Science, Pune

Brajesh Pandey
Nidhi Shrivastava

INSA, International Division
INSA, International Division



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026



Participants Details



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Utsav BANERJEE

Assistant Professor

Department of Electronic Systems Engineering
Indian Institute of Science

e-Mail: utsav@iisc.ac.in

Homepage:

<https://banerjeeutsav.github.io>, <https://labs.dese.iisc.ac.in/sinesyslab>



Dr. Utsav Banerjee received his B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology (IIT) Kharagpur in 2013, and his S.M. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT) in 2017 and 2021 respectively. He is currently an Assistant Professor in the Department of Electronic Systems Engineering at the Indian Institute of Science (IISc). He received the President of India Gold Medal from IIT Kharagpur in 2013, the Irwin and Joan Jacobs Presidential Fellowship from MIT in 2015, the Qualcomm Innovation Fellowship in 2016, the Pratiksha Trust Young Investigator Award from IISc in 2022, the ABB Research Award in 2022, the Intel Rising Star Faculty Award in 2023 and the Prof. Priti Shankar Teaching Award for Assistant Professors in Engineering from IISc in 2025.

Research Interests:

chip design, cryptography, hardware security, quantum-inspired computing, bioinformatics, energy-efficient digital circuits, embedded systems.

Representative Publications:

1. K. S. T. Ramapragada, U. Banerjee, “A 0.05mm² 1.19-to-7.34mW SQIsign-1D Isogeny-Based Post-Quantum Signature Verification Accelerator for IoT,” *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 432-434, February 2026.
2. S. Maji, U. Banerjee, S. H. Fuller, A. P. Chandrakasan, “A Threshold Implementation-based Neural Network Accelerator Securing Model Parameters and Inputs against Power Side-Channel Attacks,” *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 518-520, February 2022.
3. U. Banerjee, A. P. Chandrakasan, “A Low-Power Elliptic Curve Pairing Crypto-Processor for Secure Embedded Blockchain and Functional Encryption,” *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-2, April 2021.
4. U. Banerjee, A. Pathak, A. P. Chandrakasan, “An Energy-Efficient Configurable Lattice Cryptography Processor for the Quantum-Secure Internet of Things,” *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 46-48, February 2019.
5. U. Banerjee, C. Juvekar, A. Wright, Arvind, A. P. Chandrakasan, “An Energy-Efficient Reconfigurable DTLs Cryptographic Engine for End-to-End Security in IoT Applications,” *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 42-44, February 2018.



Efficient Hardware Acceleration for Emerging Security Applications

Dr. Utsav Banerjee
Department of Electronic Systems Engineering
Indian Institute of Science
(e-Mail: utsav@iisc.ac.in)

Hardware security has emerged as a growing concern with the advent of the Internet of Things (IoT) which consists of large networks of wireless-connected embedded devices. Although the growth of IoT has enabled novel applications, they have also become attractive targets for cyber adversaries. Securing these resource-constrained systems involves circuits, architectures and algorithms with low computation and storage overheads as well as physical attack countermeasures. One such approach is the design of efficient cryptographic hardware accelerators for IoT applications. This talk will provide an overview of design considerations and custom hardware architectures for modern public key cryptography based on elliptic curves, isogenies and lattices. ASIC implementation results will be presented, along with examples of software-hardware co-design, system-level integration and demonstration of end-to-end security protocols. This talk will summarize key results and emerging directions of research in the implementation aspects of cryptography and hardware security.

References:

1. K. S. T. Ramapragada, U. Banerjee, “miniSQI: A Compact and Low-Power SQIsign-1D Post-Quantum Digital Signature Verification Accelerator,” *IEEE Solid-State Circuits Letters*, vol. 9, pp. 238-241, August 2026.
2. K. S. T. Ramapragada, U. Banerjee, “A 0.05mm² 1.19-to-7.34mW SQIsign-1D Isogeny-Based Post-Quantum Signature Verification Accelerator for IoT,” *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 432-434, February 2026.
3. U. Banerjee, A. P. Chandrakasan, “A Low-Power BLS12-381 Pairing Crypto-Processor for Internet-of-Things Security Applications,” *IEEE Solid-State Circuits Letters*, vol. 4, pp. 190-193, October 2021.
4. U. Banerjee, A. P. Chandrakasan, “A Low-Power Elliptic Curve Pairing Crypto-Processor for Secure Embedded Blockchain and Functional Encryption,” *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-2, April 2021.
5. U. Banerjee, S. Das, A. P. Chandrakasan, “Accelerating Post-Quantum Cryptography using an Energy-Efficient TLS Crypto-Processor,” *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, October 2020.
6. U. Banerjee, T. S. Ukyab, A. P. Chandrakasan, “Sapphire: A Configurable Crypto-Processor for Post-Quantum Lattice-based Protocols,” *IACR Transactions on Cryptographic Hardware and Embedded Systems*, vol. 2019, no. 4, pp. 17-61, August 2019.
7. U. Banerjee, A. Pathak, A. P. Chandrakasan, “An Energy-Efficient Configurable Lattice Cryptography Processor for the Quantum-Secure Internet of Things,” *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 46-48, February 2019.
8. U. Banerjee, A. Wright, C. Juvekar, M. Waller, Arvind, A. P. Chandrakasan, “An Energy-Efficient Reconfigurable DTLS Cryptographic Engine for Securing Internet of Things Applications,” *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2339-2352, May 2019.
9. U. Banerjee, C. Juvekar, A. Wright, Arvind, A. P. Chandrakasan, “An Energy-Efficient Reconfigurable DTLS Cryptographic Engine for End-to-End Security in IoT Applications,” *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 42-44, February 2018.



Holger Blume

Prof. Dr.

Institute of Microelectronic Systems
Leibniz University Hannover

e-Mail: blume@ims.uni-hannover.de

Homepage: <https://www.ims.uni-hannover.de/en/>



Holger Blume is professor for architectures and systems at the Institute of Microelectronic Systems at Leibniz University Hannover.

He is one of the spokespersons of the Cluster of Excellence Hearing for All and he is one of the speakers of the Chipdesign Germany network.

His research interests are in design space exploration for algorithms and architectures for digital signal processing and corresponding chip designs using modern semiconductor technologies. Main application fields, which are addressed, are biomedical applications and highly automated driving.

- 1.) *Oberschulte, T.; Sievers, E.; Blume, H.:* "RRNS Arith Lib—Open-Source Redundant Residue Number System Arithmetics for Reliable Circuits", IEEE Open Journal of Circuits and Systems, Vol. 7, pp. 434-446, 2026, DOI: <https://doi.org/10.1109/OJCAS.2026.3717375>
- 2.) *Karrenbauer, J.; Schönwald, S.; Klein, S.; Kautz, F.; Adiloglu, K.; Kretzschmar, C.; Bruns, T.; Bluethgen, H.-M.; Blawat, M.; Benndorf, J.; Blume, H.:* "SmartHeaP- A High-level Programmable and Customized Hearing Aid System on Chip Integrated in a Research Hearing Aid Prototype", IEEE Transactions on Biomedical Circuits and Systems, oct. 2024, pp. 1-17. DOI: <https://doi.org/10.1109/TBCAS.2024.3481044>
- 3.) *Stuckenberg, T.; Rücker, M.; Gottschlich, M.; Rother, N.; Nowosielski, R. Wiese, F.; Blume, H.:* "Design and Evaluation of a 180 nm Powerline Communication ASIC for Harsh Environment", Microprocessors and Microsystems, Volume 97, March 2023, 104742, DOI: <https://doi.org/10.1016/j.micpro.2022.104742>
- 4.) *Gerlach, L.; Payá Vayá, G.; Blume, H.:* "A Survey on Application Specific Processor Architectures for Digital Hearing Aids", Journal of Signal Processing Systems, 20.3.2021, DOI: <https://doi.org/10.1007/s11265-021-01648-0>
- 5.) *Klein, S.; Rossol, L.; Venema, F.; Schönwald, S.; Karrenbauer, J.; Blume, H.:* "Noise Reduction in Hearing-Aid Processors: Traditional Methods vs. Neural Networks", 2025 IEEE 36th International Conference on Application-specific Systems, Architectures and Processors (ASAP), DOI: <https://doi.org/10.1109/ASAP65064.2025.00037>



Design of Application Specific Processors – From Medical Implants to Industrial Applications

Holger Blume

Institute of Microelectronic Systems

Leibniz University Hannover

(e-Mail: blume@ims.uni-hannover.de)

Today, every application requires that very specific constraints are met concerning the associated signal processing architectures. Typically, these parameters are power consumption, throughput rate and affordable silicon area. Therefore, classical cost metrics such as the ATE product are applied. However, these cost metrics alone do not cover the diverse requirements of modern applications. There are a lot of specific constraints, such as the maximum operating temperature, the system's latency, and its resilience to other environmental factors. Navigating the design space and identifying a suitable architecture that meets all these constraints is referred to as design space exploration. Quantitative optimization techniques must be used to identify suitable architectural approaches. Naturally, this problem also involves joint optimization across the system, architecture, and circuit levels, all the way down to the technology level.

This presentation discusses different application fields ranging from dedicated processors for ultra low power hearing aids [1, 2] to high performance AI accelerators in highly automated driving [4] or dedicated and robust processors for harsh environments in industrial or space applications [3]. For each of these application areas, the specific constraints are identified, and the designed and implemented solutions and architectures are presented.

References and Notes:

1. Karrenbauer, J.; Schönwald, S.; Klein, S.; Kautz, F.; Adiloglu, K.; Kretzschmar, C.; Bruns, T.; Bluethgen, H.-M.; Blawat, M.; Benndorf, J.; Blume, H.: "SmartHeaP- A High-level Programmable and Customized Hearing Aid System on Chip Integrated in a Research Hearing Aid Prototype", IEEE Transactions on Biomedical Circuits and Systems, oct. 2024, pp. 1-17. DOI: <https://doi.org/10.1109/TBCAS.2024.3481044>
2. Karrenbauer, J.; Schönwald, S.; Klein, S.; Blume, H.: "Enhancing a Hearing Aid Processor with ISA Extensions Supporting Flexible Fixed-Point Formats", IEEE 35th International Conference on Application-Specific Systems, Architectures and Processors, ASAP 2024, S. 176-183, DOI: <https://doi.org/10.1109/asap61560.2024.00044>
3. Hawich, M.; Rumpeltin, N.; Rücker, M.; Stuckenberg, T.; Blume, H.: "RISC-V Instruction Fetch Architecture Optimized for Harsh Environments ", International Journal of Parallel Programming 2026, Vol. 54, Article Number 9, DOI: <https://doi.org/10.1007/s10766-026-00823-9>
4. Mojumder, S.; Friedrich, S.; Matus, E.; Lüders, M.; Friedrich, M.; Renke, O.; Blume, H.; Kock, M.; Schewior, G.; Schmidt, P.; Becker, J.; Grantz, D.; Nael Fasfous, N.; AhmadiFarsani, S.; Kontopoulos, L.; Schlichtmann, U.; Benndorf, J.; Hoefer, J.; Mori, P.; Vögel, H.-J.: "ZuSE-KI-Mobil AI Chip Design Platform for Automotive and Industrial Applications", IEEE Transactions on very large scale Integration (VLSI) Systems, VOL. 33, NO. 11, November 2025, DOI: <https://doi.org/10.1109/TVLSI.2025.3603887>



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Melvin GALICIA

Postdoctoral Researcher

Institute for Communication Technologies and
Embedded Systems (ICE)
University of RWTH Aachen

e-Mail: galicia@ice.rwth-aachen.de



Homepage: <https://www.ice.rwth-aachen.de/cms/ice/Der-Lehrstuhl/Team/~bhhxzf/Melvin-Galicia-Cota/lidx/1/https://www.linkedin.com/in/melvin-galicia-287aa25a/>

I am currently working and conducting research on the next generation of computing: 'Neuromorphic computing', as a postdoctoral researcher. My work focuses on future system architectures for edge AI devices and virtual prototypes for early performance estimations. I am an experienced software engineer with a proven track record of working in the ICT industry. I am skilled in telecommunication systems: LTE, 5G, and public safety applications. I have strong engineering and management skills and a PhD in Microelectronics.

1. Patent: Inventor: Melvin Galicia. Method and apparatus for secure processing when using a hardware calculation unit, EP22207280.3
2. Galicia, M., Osman, I., Owusu-Afriyie, C. and Leupers, R.: "S3cure": Scramble, Shuffle and Shambles - Secure Deployment of Weight Matrices in Memristor Crossbar Arrays, in Association for Computing Machinery, ACM, ICONS '23: Proceedings of the 2023 International Conference on Neuromorphic Systems, Aug. 2023, doi: 10.1145/3589737.3605964
3. Melvin Galicia, Farhad Merchant, Rainer Leupers: A Parallel SystemC Virtual Platform for Neuromorphic Architectures. ISQED 2022, doi: 10.1109/ISQED54688.2022.9806235, Best paper award



Designing a Secure Compute-In-Memory Accelerator

Melvin Galicia*

Institute for Communication Technologies and Embedded Systems (ICE)

University of RWTH Aachen

(e-Mail: galicia@ice.rwth-aachen.de)

Crossbar arrays based on emerging memristor technology offer significant power savings when running ANN applications. Another advantage of this technology is that it is non-volatile, eliminating the need to load a complete ANN model from conventional memories and saving power while allowing immediate system availability. However, from a security perspective, this advantage can arguably be seen as a disadvantage, since the ANN model remains on the crossbar indefinitely and is therefore vulnerable to theft. Conversely, a disadvantage of current memristor technology is its limited write endurance. Taking these two constraints into account, we present a highly secure yet simple deployment method: 'S3cure', which does not require the encryption of individual stored values in the memristor. This avoids the need for rewriting after each decryption and also renders the extraction of the ANN model from the crossbar useless. In this methodology, the ANN model is permuted before deployment by multiplying the model weight matrices with permutation matrices. The inverse permutation vectors of these matrices then become the access key needed at runtime to correctly exploit the model.

References and Notes:

1. Melvin Estuardo Galicia, Ibrahim Jimale Osman, Christian Owusu-Afriyie, and Rainer Leupers. 2023. "S3cure": Scramble, Shuffle and Shambles - Secure Deployment of Weight Matrices in Memristor Crossbar Arrays. In Proceedings of the 2023 International Conference on Neuromorphic Systems (ICONS '23). Association for Computing Machinery, New York, NY, USA, Article 41, 1–8. <https://doi.org/10.1145/3589737.3605964>



Tanja HARBAUM

Institut für Technik der Informationsverarbeitung (ITIV)
Karlsruhe Institute of Technology (KIT)

e-Mail: harbaum@kit.edu

Homepage: https://www.itiv.kit.edu/21_3015.php



Tanja Harbaum studied Computer Science at the Karlsruhe Institute of Technology (KIT), focusing on computer architectures and robotics. Following graduation, she worked on high-energy physics experiments involving trigger systems with extreme latency requirements and researched reconfigurable microarchitectures. She completed her PhD in Electrical Engineering at KIT, and has been a team leader at the “Institut fuer Technik der Informationsverarbeitung” (ITIV) since 2019. Her research focuses on designing novel computer architectures and artificial intelligence for embedded systems. A particular focus is on hardware/software co-design, which enables fast and efficient AI execution on embedded systems. She is active in several conferences, including serving as General Chair for the IEEE International System-on-Chip Conference (SOCC) and as a TPC member for the Design Automation Conference (DAC) and the Design, Automation and Test in Europe Conference (DATE). Selected publications (from more than 50):

T. Harbaum, A. Serdyuk, F. Kreß, T. Hamann, J. Barth, P. Kämpf, F. Imbert, Y. Soullard, R. Tavenard, E. Anquetil, and J. Delahaie „KIHT: Kaligo-Based Intelligent Handwriting Teacher”, in 2024 Design, Automation & Test in Europe Conference & Exhibition (DATE), doi: 10.23919/DATE58400.2024.10546623

F. Kreß, V. Sidorenko, P. Schmidt, J. Hoefer, T. Hotfilter, I. Walter, T. Harbaum, and J. Becker „CNNParted: An open source framework forefficient Convolutional Neural Network inference partitioning in embedded systems”,in Computer Networks, vol. 229, Jun. 2023, doi: 10.1016/j.com-net.2023.109759

T. Harbaum, M. Seboui, M. Balzer, J. Becker, and M. Weber „A Content Adapted FPGA Memory Architecture with Pattern Recognition Capability for L1 Track Triggering in the LHC Environment”, in 2016 IEEE 24th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), doi: 10.1109/FCCM.2016.52

T. Harbaum, I. Topko, A. Serdyuk, I. Fürst-Walter, F. Kreß, and J. Becker, „HW/SW Co-Design for Integrated AI Systems: Challenges, Use Cases and Steps Ahead”, in 3rd Workshop on Deep Learning for IoT (DL4IoT-2024), Jan. 2024. Link: <https://hal.science/hal-04568785>

F. Lesniak, A. Gutermann, T. Harbaum, and J. Becker, „Enhanced Accelerator Design for Efficient CNN Processing with Improved Row-Stationary Dataflow,” in Proceedings of the Great Lakes Symposium on VLSI 2024, ser. GLSVLSI '24, New York, NY, USA: Association for Computing, doi: 10.1145/3649476.3658737



Hardware/Software Co-Design for Integrated AI Systems

Dr. Tanja Harbaum*

Institut für Technik der Informationsverarbeitung (ITIV)

Karlsruhe Institute of Technology (KIT)

(e-Mail: harbaum@kit.edu)

Applications of artificial intelligence (AI) are becoming increasingly important in many areas of business, science and society. Recent advances in algorithms, computer architectures and big data have enabled significant breakthroughs in a wide range of AI applications. In many domains, there is a trend to shift intelligence from the cloud to the edge. However, integrating AI systems at the edge requires powerful solutions to be developed under very tight resource constraints. While solutions that deliver very good results in the high-performance domain often exist, the use of AI approaches in embedded systems remains a major challenge. In the context of the Internet of Things (IoT), energy consumption often limits the use of machine learning methods, making tailored hardware architectures essential to meet these demands. Although effective hardware/software co-design methods have been studied for decades, they are not yet standard practice in the development of complex embedded systems, including integrated AI systems. Until now, integrated AI systems have mostly been limited to a dedicated use case and have been unable to adapt significantly to changes. This talk will explore the application of an intelligent learning device for automated handwriting, demonstrating an environment with extremely limited resources. Low-power hardware accelerators for various neural networks have been developed to distribute the complexity of the overall system between software and hardware, enabling fast and efficient AI execution. The talk will also discuss a combined evaluation of model quality and hardware performance for integrated AI systems, enabling a holistic exploration of the design space.

References and Notes:

1. Last Name, S. R.; Last Name, S. C.; Last Name, R.; Last Name, V. *Journal Name* **20XX**, vol, page XX – page XX.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Mattis HASLER

Senior Researcher

Scalable Computing Hardware
Barkhausen Institut

e-Mail: mattis.hasler@barkhauseninstitut.org

Homepage: <https://www.barkhauseninstitut.org/forschung/forschungsgruppen/scalable-computing-hardware>



Mattis Hasler has been working at the Technical University of Dresden until 2021 before starting to work for the Barkhausen Institut. He holds the degrees of Dipl.-Ing. and Dr.-Ing. both received from the mentioned university. At the Barkhausen Institut, he is member of the group for digital design. He specializes in front-end matters for system-on-chip designs and managing the EDA tooling for the group's hardware projects.

Recent development towards more collaboration with other hardware groups lead to an increased intensity in work around the ease of onboarding new developers into the local development environment. For the collaborative tape outs the groups employs once a year Mattis is responsible for orchestrating the top-level architecture and finding and resolving the challenges arising from the multi-tenancy of a project.

Research Areas

MPSoC architecture, Hardware OS Codesign, Network on Chip, EDA tool Management, Hardware Security

Publications

1. Haas, S., Hasler, M., et al. An Architectural Approach for the Secure Integration of Hardware Accelerators into a Trustworthy MPSoC Platform. In *2025 IEEE 18th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc)* (pp. 151-158). IEEE.
2. Hasler, M; Haas, S. RoadRunner: A Modularized Design and Tool Manager for Hardware Projects. In: *2025 IEEE 38th International System-on-Chip Conference (SOCC)*. IEEE, 2025. S. 1-6.
3. Hasler, M., Choc: A Communication Toolkit to Help Hardware Module Drivers Navigate SoC Architectures, 4th Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE '25), 2025



Masur - Collaborative Chip Design Platform

Dr. Mattis Hasler
Scalable Computing Hardware
Barkhausen Institut
(e-Mail: mattis.hasler@barkhauseninstitut.org)

Multi-tenant MPSoCs offer a cost-effective path for small research teams to participate in silicon fabrication by sharing tapeout resources. However, combining intellectual property (IP) from diverse contributors into a single chip introduces substantial integration challenges spanning environment compatibility, platform adaptation, physical design, and project management.

Masur is a flexible MPSoC framework designed to accommodate multiple tenants, addressing the challenges of coexistence of multiple teams and their IP in a single project.

It employs a strong isolation strategy to ensure privacy, security and safety attributes for the different tenants.

Having a strong isolation allows for a trustworthy operation of a multi-tenant MPSoC with a micro kernel operating system, like the M³ OS, developed inhouse especially for Masur.

The Masur platform allows a wide range of collaboration modes, including the import of tenant IP as hard macro as well as soft macro. It also provides a range of infrastructure modules that tenants can use. Apart from the mandatory trusted communication unit (TCU), these are among others: clock generation, power control (including measuring power of one module in isolation), BIST controllers, JTAG taps, coherent cache system, DRAM interface access.

Running a multi-tenant project also encompasses technical challenges, like for example the fact that SystemVerilog (being the de facto intermediate representation for EDA tooling) has a global namespace, which can easily lead to incompatibilities between teams.

References and Notes:

1. Haas, S., Hasler, M., et al. An Architectural Approach for the Secure Integration of Hardware Accelerators into a Trustworthy MPSoC Platform. In *2025 IEEE 18th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc)* (pp. 151-158). IEEE.



Malte Gerriet HAWICH

Dr.-Ing.

Department of Microelectronic Systems
Architecture and Systems Group
Leibniz University of Hannover

e-Mail: malte.hawich@ims.uni-hannover.de

Homepage:

<https://www.ims.uni-hannover.de/institut/personenverzeichnis/hawich>



Dr.-Ing. Malte Hawich is a researcher and chip designer specializing in digital ASIC and SoC design, processor architectures, and AI accelerators. His work ranges from high-performance RISC-V systems and integrated circuits for extreme-temperature environments to energy-efficient AI acceleration. His doctoral research resulted in the HOT-RISC-V SoC, which he brought from architecture and RTL design through physical implementation to fabricated and validated silicon; this work received the Best Paper Award at SAMOS XXV and is further presented in an accepted VLSI-SoC 2026 paper. His current research increasingly focuses on heterogeneous SoCs and AI accelerator architectures, including silicon-validated ultra-low-power AI accelerators and AI hardware for high-temperature applications.

Selected Publications

M. Hawich et al., “A Silicon-Validated High-Frequency RISC-V SoC for Extreme-Temperature Applications,” 34th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2026), to appear in VLSI-SOC 2026.

M. Hawich et al., “The HOT-RISC-V: A High-Operating-Temperature RISC-V Architecture for Extreme Conditions,” 25th International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XXV), 2025. Stamatis Vassiliadis Best Paper Award. Proceedings forthcoming.

M. Hawich, N. Rumpeltn, M. Rücker, T. Stuckenberg, and H. Blume, “RISC-V Instruction Fetch Architecture Optimized for Harsh Environments,” International Journal of Parallel Programming, vol. 54, article 9, 2026. DOI: 10.1007/s10766-026-00823-9.

S. C. Klein, M. Hawich, N. Rumpeltn, and H. Blume, “LINA: a 552 GOPS/W Lightweight Interleaver Network Accelerator ASIC for CNNs in Low-Power Hearing Aids,” Research Square, preprint, 2026. Journal manuscript under review. DOI: 10.21203/rs.3.rs-9472962/v1.



HOT-RISC-V: Architecture–Technology Co-Design for High-Performance Computing at 200 °C

Dr.-Ing, Malte Hawich
Department of Microelectronic Systems
University of Hannover
(e-Mail: malte.hawich@uni-hannover.de)

Extreme-temperature environments such as deep drilling place unusual demands on embedded processors. Beyond device-level degradation, high temperature exposes architectural bottlenecks in memories, control paths, timing closure, and the coordination of variable-latency execution units. This talk presents the development of HOT-RISC-V, a RISC-V processor and system-on-chip designed specifically around these constraints. Rather than treating temperature tolerance as a technology problem alone, the work combines silicon-on-insulator technology with architectural techniques including deep pipelining, instruction prefetching, decoupled handshakes, localized hazard management, and dedicated clock-domain organization. The presentation follows the evolution from architectural exploration and synthesis to a fabricated and experimentally evaluated chip. Particular emphasis is placed on the design trade-offs between frequency, throughput, area, power, memory latency, and implementation complexity. The goal is to provide a processor-design perspective on how architecture and circuit technology can be co-optimized to enable reliable computation in harsh environments and to discuss lessons transferable to other embedded ASICs.

References and Notes:

1. M. Hawich et al., “A Silicon-Validated High-Frequency RISC-V SoC for Extreme-Temperature Applications,” 34th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2026), to appear in VLSI-SOC 2026. M. Hawich et al., “The HOT-RISC-V: A High-Operating-Temperature RISC-V Architecture for Extreme Conditions,” 25th International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XXV), 2025. Proceedings forthcoming.
3. M. Hawich, S. C. Klein, T. Stuckenberg and H. Blume, "Improving Clock Frequencies in ASIC Designs through Semi-Automatic Register Placement and Advanced Retiming," 2024 Panhellenic Conference on Electronics & Telecommunications (PACET), Thessaloniki, Greece, 2024, pp. 1-6, doi: 10.1109/PACET60398.2024.10497079.
4. M. Hawich, J. Szücs and H. Blume, "High Temperature In-Order RISC-V Processor with Heterogeneous Pipeline and Out-of-Order Write-Back Mechanism," 2024 Kleinheubach Conference, Miltenberg, Germany, 2024, pp. 1-4, doi: 10.23919/IEEECONF64570.2024.10738940.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Manjula J

Associate Professor

Department of Electronics and Communication Engineering
SRM Institute of Science and Technology

e-Mail: manjulaj@srmist.edu.in

Homepage: <https://www.srmist.edu.in/faculty/dr-j-manjula/>



Dr. J. Manjula is an Associate Professor in the Department of Electronics and Communication Engineering at SRM Institute of Science and Technology (SRMIST), with nearly three decades of academic and teaching experience. Received Ph.D. in RF VLSI in 2015 and M.Tech. in VLSI Design in 2006, and was a Gold Medalist. Areas of interest include VLSI design, RF and analog integrated circuits, low-power and high-speed circuit design, mixed-signal ICs, and EDA-based design methodologies. Published extensively in SCI- and Scopus-indexed journals and has guided research and student projects in VLSI and related areas. Proficient in Cadence Virtuoso, Synopsys EDA Tools, and Xilinx Vivado Design Suite for IC design, synthesis, implementation, simulation, and FPGA-based system design. Professional contributions include organizing and coordinating industry-oriented training programs and workshops on VLSI, EDA tools, FPGA design, and RTL-to-GDSII implementation. And member of professional bodies including Indian Science Congress, and the Institution of Engineers (India).



Designing Energy-Efficient Mixed-Signal and RF ICs For Next-Generation Computing and Communication Systems

Dr. J. Manjula*

Department of Electronics and Communication Engineering
SRM Institute of Science and Technology
(e-Mail: manjulaj@srmist.edu.in)

The rapid development of 5G/6G networks, edge artificial intelligence, intelligent sensing, high-speed data processing, and emerging computing platforms requires integrated circuits that deliver high performance with low energy consumption. Mixed-signal and radio-frequency (RF) ICs provide the essential interface between the physical world and digital systems, making their efficiency critical to overall system performance. This work focuses on energy-efficient mixed-signal and RF circuit design, addressing the trade-offs among power, speed, noise, linearity, accuracy, bandwidth, and robustness. Key RF blocks, including low-noise amplifiers, mixers, voltage-controlled oscillators, phase-locked loops, and variable-gain amplifiers, along with mixed-signal blocks such as comparators, ADCs, and DACs, are considered. A high-speed, low-power CMOS dynamic comparator is highlighted as a case study. The EDA-based methodology covers circuit design, transistor-level optimization, PVT and Monte Carlo analysis, layout, parasitic extraction, and post-layout verification. Emerging opportunities in AI-assisted design, advanced CMOS, mmWave/6G circuits, and energy-efficient data converters are also discussed.

References and Notes:

1. Brindha, K.; Manjula, J. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields* **2024**, 37, e3263.
2. Brindha, K.; Manjula, J. *AEU – International Journal of Electronics and Communications* **2024**, 187, 155550.
3. Razavi, B. *IEEE Solid-State Circuits Magazine* **2015**, 7, 12–17.
4. Lei, K.-M.; Mak, P.-I.; Martins, R. P. *Analog Integrated Circuits and Signal Processing* **2013**, 77, 277–284.
5. Figueiredo, P. M.; Vital, J. C. *IEEE Transactions on Circuits and Systems II: Express Briefs* **2006**, 53, 541–545.
6. Wang, Y.-T.; Razavi, B. *IEEE Journal of Solid-State Circuits* **2000**, 35, 308–317.
7. Zhuang, H.; Tang, H.; Liu, X. *IEEE Transactions on Circuits and Systems II: Express Briefs* **2020**, 67, 2923–2927.
8. Yoshioka, K. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* **2021**, 29, 2143–2152.
9. Rahman, R. L. F.; Reaz, M. B. I.; Yin, C. C.; Marufuzzaman, M.; Rahman, M. A. *The Scientific World Journal* **2014**, 2014, 508571.
10. Schinkel, D.; Mensink, E.; Klumperink, E.; van Tuijl, E.; Nauta, B. *IEEE Journal of Solid-State Circuits* **2007**, 42, 1767–1776.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Kapil Jainwal
Assistant Professor

Department of Electrical Engineering
IIT Hyderabad, India

e-Mail: kapiljainwal@ee.iith.ac.in

Homepage: <https://iith.ac.in/ee/kapiljainwal/>



Dr. Kapil Jainwal is an Assistant Professor in the Department of Electrical Engineering at the Indian Institute of Technology Hyderabad (IIT Hyderabad). His research interests include analog/digital integrated-circuit design, CMOS image sensors, 2D/3D vision sensors, Time-of-Flight (ToF) based 3D cameras, LiDAR, and event-based cameras. His research program focuses on the development of low-noise, high-dynamic-range and high-speed CMOS imaging systems, as well as emerging intelligent vision architectures.

He received his Ph.D. from IIT Delhi, where he worked on on-chip CMOS image sensors. Before joining IIT Hyderabad, he served as an Assistant Professor in the Department of Electrical Engineering at IIT Bhilai and gained industry experience with Samsung Research and Development in its analog design team. He also carried out research at the University of California, Riverside, and received his Master's degree from IIT Bombay and Bachelor's degree in Engineering from SGSITS Indore. He joined IIT Hyderabad as an Assistant Professor in June 2023.

Research Areas

Analog/Digital IC Design, CMOS Image Sensors, 2D/3D Vision Sensors and ToF Cameras, LiDAR and Direct Time-of-Flight Imaging, Event-Based and Bio-Inspired Vision Sensors, Low-Noise and High-Dynamic-Range Imaging

Representative Publications

1. P. Philip, K. Jainwal, A. van Schaik, and C. S. Thakur, "Tau-Cell-Based Analog Silicon Retina With Spatio-Temporal Filtering and Contrast Gain Control," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 18, no. 2, pp. 423–437, April 2024. DOI: 10.1109/TBCAS.2023.3332117.
2. K. Jainwal and M. Sarkar, "A 280- μ V Temporal Noise, 76-dB Dynamic Range CMOS Image Sensor With an In-Pixel Chopping-Based Low-Frequency Noise Reduction Technique," *IEEE Transactions on Electron Devices*, vol. 70, no. 3, pp. 1134–1142, March 2023. DOI: 10.1109/TED.2023.3236911.
3. K. Jainwal, C. Anand, and M. Sarkar, "1/f Noise Reduction Using In-Pixel Chopping in CMOS Image Sensors," *IEEE Solid-State Circuits Letters*, vol. 1, no. 6, pp. 146–149, July 2018.



Design challenges of a CMOS Image sensor

Dr. Kapil Jainwal

Department of Electrical Engineering
Indian Institute of Technology Hyderabad, India
(e-Mail: kapiljainwal@gmail.com)

CMOS image sensors have become a key enabling technology for modern imaging systems, finding applications in smartphones, autonomous vehicles, industrial inspection, biomedical imaging, robotics, and machine vision. The rapid evolution of these applications is driving increasingly stringent requirements for higher resolution, faster readout, wider dynamic range, lower noise, reduced power consumption, and improved image quality, while maintaining low cost and compact form factor. Meeting these requirements simultaneously presents significant challenges at both the pixel and system levels.

This talk will discuss the fundamental design challenges involved in developing high-performance CMOS image sensors, with emphasis on pixel architecture, noise, sensitivity, dynamic range, conversion gain, charge handling capacity, dark current, and readout speed. The trade-offs between key performance parameters will be explored, highlighting how improvements in one metric often introduce limitations in others. The talk will further examine circuit-level challenges associated with column readout, analog-to-digital conversion, correlated double sampling, high-speed operation, power management, and on-chip signal processing.

Beyond conventional imaging, emerging applications such as high-dynamic-range imaging, 3D sensing, LiDAR, and event-based vision demand new sensor architectures that integrate sensing, computation, and intelligence closer to the pixel. The talk will therefore also highlight emerging approaches for overcoming conventional CMOS image sensor limitations through advanced pixel architectures, 3D integration, in-pixel/near-pixel processing, and computational imaging. Finally, the talk will discuss the key technology and circuit design trade-offs that will shape the next generation of CMOS image sensors.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Dr. Shahanawaz Kamal
Senior Researcher

Radio Frequency Design Enablement Group
Barkhausen Institut, Dresden, Germany

e-Mail: shahanawaz.kamal@barkhauseninstitut.org

Homepage: <https://www.barkhauseninstitut.org/en/research/research-groups/rf-design-enablement>



Shahanawaz Kamal was born in Mumbai, India, in 1991. He received the Diploma degree in electronics and telecommunication engineering from the Maharashtra State Board of Technical Education, India, in 2010; the B.E. and M.E. degrees in electronics and telecommunication engineering from the University of Mumbai, India, in 2013 and 2017, respectively; and the Ph.D. degree in antenna and propagation from Universiti Sains Malaysia, Malaysia, in 2022. He was an In-Building Solution (IBS) Engineer at Vedang Cellular Services, India, in 2014. He was a Visiting Lecturer with M.H. Saboo Siddik Polytechnic, India, in 2016. He was affiliated as a Graduate Research Assistant with Universiti Sains Malaysia, Malaysia, from 2019 to 2022. He has been a Senior Researcher with Barkhausen Institut, Germany, since 2022. He has authored over 39 papers, with more than 26 Web of Science (WoS) Core Collection publications, since 2017. He is an inventor of a German patent “Antenne, antennenstruktur und vorrichtung,” granted in 2025. He has reviewed over 231 papers for more than 31 WoS journals, since 2018. He is a recipient of the 2026 IEEE ANTENNAS AND WIRELESS PROPAGATION LETTERS Outstanding Reviewer Award, ranking in the top 61 of over 1,800 reviewers. He has guest-edited a special issue of *Sensors* journal, in 2024. His research interests include concept-to-prototype development of impedance matching networks, metamaterials, reflecting surfaces, and antennas based on circuit boards, wafers, sheet metals, novel materials, dielectric resonators, and artificial intelligence for the IEEE VHF-to-W bands.

- [1] S. Kamal and P. Sen, “Printed multiple input multiple output antennas powered by passive metamaterial and defected ground for diverse sixth generation applications,” *Nat. Sci. Rep.*, 15(1):22723, Jul. 2025.
- [2] S. Kamal and P. Sen, “Microstrip-ministered proximity-coupled stacked dual-port antenna for 6G applications,” *IEEE Access*, 12:2817-2829, Jan. 2024.
- [3] S. Kamal, et al., “Enabling MIMO antenna miniaturization and wide circular polarization coverage by amalgamation of a dielectric strip between meandered traces and slotted ground,” *IEEE Antennas Wirel. Propag. Lett.*, 21(9):1901-1905, Jun. 2022.
- [4] M. Omar, I. Zubir, S. Kamal, and M. Ain, “A tri-hybrid of Al_2O_3 - SiO_2 - $MgZrO_3$ stair shaped half-cylindrical dielectric resonator antenna (SHCDRA) for wideband wireless communication systems,” *Elsevier Eng. Sci. Technol.*, 35:101187, Jun. 2022.
- [5] S. Kamal, et al., “Wheel-shaped miniature assembly of circularly polarized wideband microstrip antenna for 5G mmWave terminals,” *Elsevier Alex. Eng. J.*, 60(2):2457-2470, Apr. 2021.



Shaping the future of wireless connectivity with transceiver and antenna chips co-design

Dr. Shahanawaz Kamal
Senior Researcher
Radio Frequency Design Enablement Group
Barkhausen Institut, Dresden, Germany
(e-Mail: shahanawaz.kamal@barkhauseninstitut.org)

Future wireless systems demand the co-design of transceiver and antenna chips. Traditional, isolated development methods limit overall system capacity and cannot meet the size and performance requirements of compact communication, radar, and integrated sensing and communication systems. The presentation will highlight recent breakthroughs in integrated circuit and antenna co-design, covering key technological aspects and performance evaluations. Subsequently, the national and international research projects of the Radio Frequency Design Enablement Group at Barkhausen Institut in Germany will be presented. The track record of group will then be demonstrated by highlighting successful tapeout, physical implementation, hardware validation, and publication records in the development of integrated circuits and antennas from 6 GHz to 60 GHz spectrum. Furthermore, the manufacturing and characterization facilities available at the in-house laboratory will be revealed. Notable circuit and system-level designs and/or results will be presented. Finally, potentials for cooperation in integrated antenna co-design for future wireless systems will be discussed.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Sashank Krishnamurthy
Assistant Professor

Department of Electrical Engineering
Indian Institute of Technology Madras

e-Mail: sashank@ee.iitm.ac.in

Homepage: [Sashank Krishnamurthy](http://SashankKrishnamurthy)



Sashank Krishnamurthy was born in India in 1993. He received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Madras, Chennai, India, in 2015, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, CA, USA, in 2020. From 2021 to 2026, he was a Research Scientist with Intel Labs, Hillsboro, OR, USA. He has also been a Visiting Lecturer at the University of California, Berkeley. Since May 2026, he has been with the Indian Institute of Technology Madras, where he is an Assistant Professor of Electrical Engineering. His research interests include analog, mixed-signal, RF, and millimeter-wave circuit techniques for next-generation wireless, wireline, and optical communication systems.

Selected Publications:

1. S. Krishnamurthy and A. M. Niknejad, "Design and Analysis of Enhanced Mixer-First Receivers Achieving 40-dB/decade RF Selectivity," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 5, pp. 1165-1176, May 2020.
2. S. Krishnamurthy and A. M. Niknejad, "Synthesis and Design of Enhanced N-Path Filters With 60-dB/decade RF Selectivity," in *IEEE Solid-State Circuits Letters*, vol. 3, pp. 522-525, 2020.
3. S. Krishnamurthy and A. M. Niknejad, "An Enhanced Mixer-First Receiver With Distortion Cancellation, Achieving 80-dB/decade RF Selectivity and +8-dBm B1dB for Adjacent Channel Blockers," in *IEEE Solid-State Circuits Letters*, vol. 4, pp. 64-67, 2021.
4. S. Krishnamurthy, L. Iotti, and A. M. Niknejad, "Design of High-Linearity Mixer-First Receivers for mm-Wave Digital MIMO Arrays," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 11, pp. 3375-3387, Nov. 2021.
5. S. Gupta, S. Krishnamurthy, A. Ravi, O. Degani and A. Natarajan, "Analysis and Design of Channel-Selective, Bandwidth Reconfigurable, Wideband Low Noise Amplifier With Dual-Frequency N-Path Filters," in *IEEE Transactions on Microwave Theory and Techniques*.
6. S. Krishnamurthy *et al.*, "A 4×50 Gb/s 2.9-pJ/b NRZ VCSEL-Based Co-Packaged Optical Link With Fiber Termination," in *IEEE Journal of Solid-State Circuits*, vol. 61, no. 5, pp. 2086-2101, May 2026.
7. S. Mondal, S. Krishnamurthy *et al.*, "A 108 Gb/s PAM-4 VCSEL-Based Direct-Drive Optical Engine for Co-Packaged Optics Applications," in *IEEE Journal of Solid-State Circuits*, vol. 61, no. 1, pp. 33-46, Jan. 2026.
8. S. Krishnamurthy, S. Mondal *et al.*, "50-GBaud+ VCSEL-Based Co-Packaged Optical Links: An Overview of Circuits and Systems," *2026 IEEE Custom Integrated Circuits Conference (CICC)*, Seattle, WA, USA, 2026, pp. 1-8.
9. S. Mondal, S. Krishnamurthy *et al.*, "A 48Gb/s/lane 1.24Tb/s/mm UCIE-Compliant Die-to-Die Link Over 30mm Standard Package," *2026 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2026, pp. 134-136.



Higher-Order N-Path Filters for Next-Generation Wireless Front Ends

Dr. Sashank Krishnamurthy
Department of Electrical Engineering
Indian Institute of Technology, Madras
(e-Mail: sashank@ee.iitm.ac.in)

As wireless spectrum becomes increasingly congested, RF front ends require high selectivity across a growing number of frequency bands. Today, this selectivity is provided by multiple acoustic filters, increasing front-end area, complexity, and cost. Through their inherent property of impedance translation, N-path filters enable tunable RF bandpass filtering through simple tuning of the LO frequency, offering a promising pathway toward integrated implementation of highly selective RF filtering in CMOS. This talk will present our work on improving the RF selectivity of N-path filters from 20 dB/decade in conventional topologies to 40, 60, and 80 dB/decade using higher-order driving-point impedances. We also discuss frequency staggering as an alternative approach to realizing higher-order N-path filters and present measurement results from several prototype integrated circuits demonstrating both approaches. Finally, we will discuss key challenges toward programmable, integrated RF filtering and the extension of these techniques to higher frequencies in the emerging 6G-FR3 bands.

References and Notes:

1. S. Krishnamurthy and A. M. Niknejad, "Design and Analysis of Enhanced Mixer-First Receiver Achieving 40-dB/decade RF Selectivity," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 5, pp. 1165-1176, May 2020, doi: 10.1109/JSSC.2019.2956887.
2. S. Krishnamurthy and A. M. Niknejad, "Synthesis and Design of Enhanced N-Path Filters With 60-dB/decade RF Selectivity," in *IEEE Solid-State Circuits Letters*, vol. 3, pp. 522-525, 2020, doi: 10.1109/LSSC.2020.3035962.
3. S. Krishnamurthy and A. M. Niknejad, "An Enhanced Mixer-First Receiver With Distortion Cancellation, Achieving 80-dB/decade RF Selectivity and +8-dBm B1dB for Adjacent Channel Blockers," in *IEEE Solid-State Circuits Letters*, vol. 4, pp. 64-67, 2021, doi: 10.1109/LSSC.2021.3059588.
4. S. Gupta, S. Krishnamurthy, A. Ravi, O. Degani and A. Natarajan, "Analysis and Design of Channel-Selective, Bandwidth Reconfigurable, Wideband Low Noise Amplifier With Dual-Frequency N-Path Filters," in *IEEE Transactions on Microwave Theory and Techniques*, doi: 10.1109/TMTT.2026.3711569.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Lukas KRUPP

Postdoctoral Researcher

Department of Microelectronic Systems Design
RPTU University Kaiserslautern-Landau

e-Mail: lukas.krupp@rptu.de

Homepage: <https://eit.rptu.de/fgs/ems/mitarbeiter/lukas-krupp>



Lukas Krupp received his B.Sc. and M.Sc. degrees in Electrical and Computer Engineering from the Technical University of Kaiserslautern, Germany, in 2018 and 2019, respectively, specializing in embedded systems. He received his Dr.-Ing. degree from the University of Duisburg-Essen in 2023, with research conducted at the Fraunhofer Institute for Microelectronic Circuits and Systems IMS and a focus on embedded AI. Since 2024, he has been a Postdoctoral Researcher in the Microelectronic Systems Design research group at RPTU University Kaiserslautern-Landau. His current research focuses on digital signal processing and machine learning hardware as well as AI-based methods for electronic design automation.

Krupp, L.; Groß, M.; Graichen, M.; Ulrich, K.; and Wehn, N. “Energy-Efficient Visual Inspection with FFT-Based CNNs and Adaptive Floating-Point Quantization.” Accepted for publication in: 2026 International SoC Design Conference (ISOCC). 2026. Preprint: arXiv:2608.19837 [cs.AR]. 2026.

Krupp, L.; Venn, M.; and Wehn, N. “From RTL to Prompt Coding: Empowering the Next Generation of Chip Designers through LLMs.” In: 2026 IEEE International Symposium on Circuits and Systems (ISCAS). 2026.

Krupp, L.; Schöffel, M.; Biehl, E.; and Wehn, N. “CRADLE: Conversational RTL Design Space Exploration with LLM-based Multi-Agent Systems.” In: 2025 International SoC Design Conference (ISOCC). 2025.

Krupp, L.; O’Connor, I.; Benini, L.; Studer, C.; Rodrigues, J.; and Wehn, N. “Improving Chip Design Enablement for Universities in Europe – A Position Paper.” In: 2025 Design, Automation & Test in Europe Conference (DATE). 2025.

Wulfert, L.; Kühnel, J.; Krupp, L.; Viga, J.; Wiede, C.; Gembaczka, P.; and Grabmaier, A. “AlfES: A Next-Generation Edge AI Framework.” In: IEEE Transactions on Pattern Analysis and Machine Intelligence (TPAMI). 2024.

Krupp, L.; Wiede, C.; Friedhoff, J.; and Grabmaier, A. “Explainable Remaining Tool Life Prediction for Individualized Production using Automated Machine Learning.” In: Sensors. 2023.



Hardware for AI and AI for Hardware Design – From Edge Intelligence to Agentic Design Automation

Dr. Lukas Krupp

Department of Microelectronic Systems Design

RPTU University Kaiserslautern-Landau

(e-Mail: lukas.krupp@rptu.de)

Artificial intelligence is transforming both how computing hardware is used and how it is designed. This talk explores this bidirectional relationship, spanning hardware for AI and AI for hardware design. Starting from embedded perception AI, it shows how established optimization methods across applications, models, software, architectures, and hardware platforms have enabled efficient intelligence on resource-constrained devices and made AI pervasive in embedded systems [1]-[6]. Building on these foundations, the talk turns to generative and agentic AI as new tools for hardware and system design, including RTL generation, verification, optimization, and design space exploration. These capabilities can accelerate design and lower barriers to hardware development [7], [8]. Looking ahead, the central challenge shifts toward physical AI systems, whose demanding requirements for performance, efficiency, autonomy, and integration will require tighter co-design. Generative and agentic AI can become key enablers for meeting the requirements of these complex, intelligent physical systems by extending proven embedded optimization methods.

References and Notes:

1. Krupp, L.; Wiede, C.; Friedhoff, J.; and Grabmaier, A. “Explainable Remaining Tool Life Prediction for Individualized Production Using Automated Machine Learning.” In: MDPI Sensors. Vol. 23, no. 20. 2023.
2. Krupp, L.; Wiede, C.; Friedhoff, J.; and Grabmaier, A. “A Cognitive Sensor System Architecture for the Monitoring of Flexible Machining Systems.” In: 2023 IEEE SENSORS. 2023, pp. 1–4.
3. Hoyer, I.; Berg, O.; Krupp, L.; Utz, A.; Wiede, C.; and Seidl, K. “Hardware Accelerators for a Convolutional Neural Network in Condition Monitoring of CNC Machines.” In: 2023 IEEE SENSORS. 2023, pp. 1–4.
4. Krupp, L.; Stahlschmidt, R.; and Wehn, N. “Security Risks in Machining Process Monitoring: Sequence-to-Sequence Learning for Reconstruction of CNC Axis Positions.” In: 2026 IEEE International Symposium on Artificial Intelligence for Instrumentation and Measurement (AI4IM). 2026, pp. 1–6.
5. Krupp, L.; Wiede, C.; and Grabmaier, A. “Approximate Fast Fourier Transform-Based Preprocessing for Edge AI.” In: 2022 IEEE 27th International Conference on Emerging Technologies and Factory Automation (ETFA). 2022, pp. 1–8.
6. Wulfert, L.; Kühnel, J.; Krupp, L.; Viga, J.; Wiede, C.; Gembaczka, P.; and Grabmaier, A. “AlfES: A Next-Generation Edge AI Framework.” In: IEEE Transactions on Pattern Analysis and Machine Intelligence. Vol. 46, no. 6. 2024, pp. 4519–4533.
7. Krupp, L.; Schöffel, M.; Biehl, E.; and Wehn, N. “CRADLE: Conversational RTL Design Space Exploration with LLM-Based Multi-Agent Systems.” In: 2025 22nd International SoC Design Conference (ISOCC). 2025.
8. Krupp, L.; Venn, M.; and Wehn, N. “From RTL to Prompt Coding: Empowering the Next Generation of Chip Designers through LLMs.” In: 2026 IEEE International Symposium on Circuits and Systems (ISCAS). 2026, pp. 3768–3772.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Abhishek, Kumar
Assistant Professor

Department of Electrical Engineering
Indian Institute of Technology Hyderabad

e-Mail: akumar@ee.iith.ac.in

Homepage: <https://people.iith.ac.in/akumar>



Abhishek Kumar received the M.E. degree in microelectronics from Indian Institute of Science Bangalore, India, in 2011, and the Ph.D. degree from IIT Madras, India, in 2018. He is currently an Assistant Professor with IIT Hyderabad, India. He completed a five-month internship with Qualcomm India Pvt., Ltd., Bengaluru, in 2014, where he designed VCO for cellular transceiver IC. His research interests include wireless circuits and systems.

Few publications:

1. R. Kiran and A. Kumar, Passive FSK Backward Telemetry with Simultaneous Power and Data Transfer Using a Self-Oscillating Inductive Link, in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 73, no. 6, pp. 4398-4408, June 2026.
2. N.V. Sonuanirudha and A. Kumar, A self-calibrating 1-bit phase shifter for reflected array antennas, Indian Patent 588193, Apr 2026.
3. H.S.T. Tammiseti and A. Kumar, A FREQUENCY DIVISION DUPLEXER (FDD) TO FACILITATE WIDEBAND ISOLATION OF TRANSMITTING AND RECEIVING FREQUENCY, Indian Patent 557058, Dec 2024.
4. M. Kadam and A. Kumar and S. Aniruddhan, A 28GHz Reflective-Type Transmission-Line-Based Phase Shifter, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 12, 2020.
5. A. Kumar and S. Aniruddhan, A 2.5-GHz CMOS full-duplex front-end for asymmetric data networks, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 10, 2018.



In-Band Full-Duplex Receiver Using Self-Interference Signal for Downconversion

Dr. Abhishek Kumar
Department of Electrical Engineering
Indian Institute of Technology Hyderabad
(e-Mail: akumar@ee.iith.ac.in)

This work presents a full-duplex (FD) integrated receiver for sub-GHz IoT links that directly samples the RF signal at the antenna interface by exploiting an inherent voltage-to-delay conversion in an FD system. The target application is a short-range sub-GHz IoT gateway or hub that operates as a friendly jamming receiver: while it receives uplink data from nearby sensors, it simultaneously transmits a strong signal in the same 0.3-1GHz band. An off-chip electrical-balance duplexer (EBD) provides antenna-domain isolation, and the proposed mixer-less architecture suppresses self-interference (SI) without on-chip RF, analog, or digital cancellers. Fabricated in a 65nm CMOS process, the receiver is tunable from 0.3-1GHz, occupies a compact 0.0125 mm² active core area, and consumes 26mW from a 1.2V supply while supporting a 10MHz signal bandwidth.

References:

1. Tammiseti, H. S. T.; Kumar, A. "TIMING-DOMAIN RECEIVER APPARATUS AND METHOD OF EXTRACTING TARGET-RELATED INFORMATION", *Indian Patent Application Number 202641094471* **2026**.
2. Kumar, A.; Ganti, R. K.; Aniruddhan, S. "A Same-Channel Full-Duplex Receiver Using Direct RF Sampling", *2018 IEEE International Symposium on Circuits and Systems (ISCAS)* **2018**.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Raveesh, Magod
Assistant Professor

Department of Electrical Engineering
Indian Institute of Technology Madras

e-Mail: raveesh@ee.iitm.ac.in

Homepage: <https://www.linkedin.com/in/raveeshmagod/>



Raveesh Magod joined the Integrated Circuits and Systems group in the Department of Electrical Engineering, IIT Madras, as an Assistant Professor in October 2025. He received his M.S. and Ph.D. degrees in Electrical Engineering from Arizona State University, Tempe, AZ, USA, in 2014 and 2018, respectively. Before joining IIT Madras, he worked as a Power Management R&D Engineer at Kilby Labs, Texas Instruments (TI), Dallas, TX, USA, from December 2017. At Kilby labs, he developed a wide range of power converter products, including nano-power voltage regulators, high power-density DC-DC converters, GaN power modules, resonant converters, and hybrid converters. From 2015 to 2016, he was an Analog Design Intern at TI, Tucson, AZ, USA, where he worked on low-power voltage supervisors and low quiescent-current LDOs.

He holds 9 granted or pending U.S. patents and has authored over 20 papers and presentations in reputed international journals and conferences. He was the co-recipient of A.K. Chowdhary Best Paper award at the International Conference on VLSI Design, 2021. He is currently serving as the Chair of the has served as the Power Management Subcommittee for the IEEE Custom Integrated Circuits Conference (CICC). He has served as a Senior Associate Editor for the IEEE Transactions on Circuits and Systems – II (TCAS-II) and as a technical program committee member for the International Workshop on Power Supply on Chip (PwrSoC).

His current research interests include high-voltage and high power-density DC-DC converters and power modules, GaN/SiC based power modules, isolated power transfer and low-power voltage regulators.



Powering the AI Revolution – GaN based Power Modules for next-generation Data Centers

Dr. Raveesh Magod
Department of Electrical Engineering
Indian Institute of Technology Madras
(e-Mail: raveesh@ee.iitm.ac.in)

The rapid expansion of megawatt-scale AI workloads demands high-efficiency, high-density power delivery architectures. To deliver this high power without inflating supply current, the industry is transitioning to higher input supply voltages (400V to 800V). This high-voltage power path relies on multi-stage conversion, stepping down to intermediate bus voltages (traditionally 54V, with a trend toward lower levels) before converting directly to the sub-1V core voltage. With clear figure-of-merit advantages over silicon FETs, GaN technology directly addresses the dual requirements of higher supply voltage and superior conversion efficiency. However, fully unlocking GaN's fast, low-loss switching requires co-packaging GaN FETs with silicon driver + controller dies to minimize parasitic inductance. Furthermore, high-voltage operation necessitates moving beyond traditional converter topologies toward multi-level architectures, optimizing the use of 40V–650V rated GaN power devices.

This talk explores current data center rack power architectures, covering main, intermediate bus, and point-of-load (PoL) converters. We will examine circuit topologies and dive into the specific GaN power modules enabling these systems. Key design considerations and trade-offs for gate-driver and control-circuit will be addressed. Finally, the presentation highlights cutting-edge research showing how advanced GaN modules are shifting power delivery toward high-voltage, high-density architectures—specifically targeting 800V supply inputs.

References and Notes:

1. Samuel Defaz, Yang Li, Abdul Muneeb, Raveesh Magod, Xin Zhang and Fang Luo, “Optimization of GaN-Based High-Current Low-Voltage Two-Stage Converter with Fully 3D Embedded Structure,” *IEEE APEC*, 2026
2. R. Magod, S. Chakraborty and S. Jha, “Switch controller with resonant gate driver,” *US patent (Pending)*
3. R. Magod, et. al., “Adjustable power FET driver,” *US patent (Pending)*
4. LMG365 family datasheet



Saravana Kumar, Manivannan
Assistant Professor

Dept. of Electronics & Communication Engineering,
IIT Roorkee

e-Mail: saravana.kumar@ece.iitr.ac.in

Homepage: [Saravana Kumar's webpage](#)



Dr. Saravana Kumar received the B.E. degree in Electronics and Communication Engineering from the Madras Institute of Technology, Anna University, Chennai, in 2009, and the M.Tech. degree from the Indian Institute of Technology Delhi, New Delhi, in 2011. From 2011 to 2014, he was a Design Engineer with Analog Devices, Bengaluru, India, where he worked on high speed chip-to-chip serial link communication. He obtained his PhD degree from the Indian Institute of Technology Madras, Chennai, in 2021, in the area of data-converter design. He also served as a Senior Project Officer in the Centre for Industrial Consultancy and Sponsored Research (IC & SR), IIT Madras, where he worked on high performance analog filters. He is now an Assistant Professor in the Department of Electronics and Communication Engineering at IIT Roorkee. His broad research areas are high performance and high bandwidth data converter design.

Representative publications:

- M. Shukla, S. K. Dey, A. Dasgupta and S. Manivannan, "Identifying Design Challenges in Analog Circuits Due to Device Nonidealities at Cryogenic Temperatures," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 45, no. 2, pp. 751-755, Feb. 2026, doi: 10.1109/TCAD.2025.3585808.
- S. Lalithamma and S. Manivannan, "A Chopper-Stabilized Bandgap Reference with a Double-Sampled FIR Filter in 180-nm CMOS," *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, Singapore, Singapore, 2024, pp. 1-5, doi: 10.1109/ISCAS58744.2024.10558104.
- S. Pavan, S. Manivannan and N. Basavaraj, "Analysis and Design of Wideband Filtering ADCs Using Continuous-Time Pipelining," in *IEEE Journal of Solid-State Circuits*, vol. 59, no. 1, pp. 268-281, Jan. 2024, doi: 10.1109/JSSC.2023.3276633.
- S. Manivannan and S. Pavan, "Improved Continuous-Time Delta-Sigma Modulators with Embedded Active Filtering," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 11, pp. 3778-3789, Nov. 2020, doi: 10.1109/TCSI.2020.3013006.



Demystifying Quantum Computing: A Circuit-Level Approach to Silicon Spin Qubits

Dr. Saravana Kumar Manivannan

Department of Electronics and Communication Engineering

Indian Institute of Technology Roorkee

(e-Mail: saravana.kumar@ece.iitr.ac.in)

Quantum computing, though often perceived as complex, can be explained using concepts familiar to circuit designers. Unlike classical bits, which represent either 0 or 1, qubits can occupy multiple states through superposition and exhibit correlations through entanglement. Silicon electron spin qubits are a promising platform for realizing future quantum processors, potentially requiring thousands of qubits integrated on a single silicon die. Developing such systems also requires cryogenic CMOS circuits for qubit control and readout, including RF blocks such as voltage-controlled oscillators (VCOs), low-noise amplifiers (LNAs), and mixers. For efficient circuit design and co-simulation, a practical qubit model based on fundamental circuit elements is highly valuable. This talk introduces the basic principles of qubits and gradually develops an intuitive circuit-level model of a silicon spin qubit. The resulting model can be incorporated into circuit simulations, providing analog designers with a bridge between quantum concepts and conventional RFIC design methodologies.



Christoph Niemann

Postdoctoral Researcher

University of Rostock, Germany
Institute of Applied Microelectronics
and Computer Engineering

e-Mail: christoph.niemann@uni-rostock.de

Homepage: <https://www.imd.uni-rostock.de/team/mitarbeitende/persoennliche-seiten/christoph-niemann/>



Christoph Niemann is with the Institute of Applied Microelectronics and Computer Engineering at the University of Rostock, Germany. His research interests include adaptive voltage scaling on FPGAs, approximate computing for FPGAs, low-power hardware for electrically active implants, and heterogeneous virtual prototypes for smart sensor systems.

He received his Ph.D. from the University of Rostock in 2023 for his thesis "Contributions to Improve the Energy Efficiency of FPGA-based Applications". He holds a Master's degree in Electrical Engineering and a Bachelor's degree in Engineering Management from the same university, and carried out research at the Universidade Federal de Minas Gerais, Belo Horizonte, Brazil.

He is co-principal investigator of subproject B03 in the DFG Collaborative Research Centre 1270 ELAINE, and co-authored the proposal for DI-HYPRSENSE, funded by the BMFTR under the DE:Sign Challenge call.

Representative Publications

1. C. Niemann, M. Rethfeldt, and D. Timmermann, "A Novel Strategy for Flexible Placement and Routing of AVS Sensors on FPGAs," in *Proc. 33rd International Conference on Field-Programmable Logic and Applications (FPL)*, Gothenburg, Sweden, pp. 339–344, Sept. 2023. DOI: 10.1109/FPL60245.2023.00058.
2. C. Niemann, M. Ali, O. U. Shah, J. Heller, and D. Timmermann, "Sensor Based Adaptive Voltage Scaling on FPGAs: Calibration and Parametrization," *Integration – the VLSI Journal*, vol. 75, pp. 30–39, Nov. 2020. DOI: 10.1016/j.vlsi.2020.05.006.
3. C. Niemann, M. Rethfeldt, and D. Timmermann, "Approximate Multipliers for Optimal Utilization of FPGA Resources," in *Proc. 24th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*, Vienna, Austria, pp. 1–6, Apr. 2021. DOI: 10.1109/DDECS52668.2021.9417027.
4. F. Plocksties, C. Niemann, M. Fauser, A. Storch, D. Timmermann, and C. Haubelt, "STELLA+: Expanding the Research Potential for Long-Term Deep Brain Stimulation Studies in Freely-Moving Rodents," in *Proc. 18th International Joint Conference on Biomedical Engineering Systems and Technologies (BIODEVICES)*, vol. 1, Porto, Portugal, pp. 74–87, Feb. 2025. DOI: 10.5220/0013305200003911



Tailoring Adaptive Voltage Scaling to the Constraints of FPGAs

Dr. Ing Christoph Niemann
Institute of Applied Microelectronics and Computer Engineering
University of Rostock
(e-Mail: christoph.niemann@uni-rostock.de)

Digital VLSI systems are conventionally designed with generous guard bands to absorb variations in process, temperature, aging, and supply-voltage noise, at the cost of energy efficiency. Adaptive Voltage Scaling (AVS) instead uses runtime information in a closed control loop to adjust the supply voltage to actual operating conditions, shrinking the guard band. While AVS is well-established for high-end chips, its application to FPGAs remains very limited. This talk shows how AVS can be tailored to the specific constraints of FPGAs, whose lack of a fixed, known application design at production time, combined with their flexibility and short time-to-market, sets them apart from ASICs. Starting from prior sensor-based AVS approaches, three challenges are addressed: sensor calibration, sensor placement, and sizing a residual guard band. A prototype evaluation on five identical FPGA boards achieved an average supply voltage reduction of 21%, which in turn cut energy consumption by 51–66%.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Shanthi PAVAN

NT Alexander Institute Chair Professor; Dean (Academic Research)

Department of Electrical Engineering
Indian Institute of Technology Madras

e-Mail: shanthi@ee.iitm.ac.in

Homepage: <https://www.ee.iitm.ac.in/shanthi/>



Shanthi Pavan received the B.Tech. degree in electronics and communication engineering from the Indian Institute of Technology Madras in 1995, and the M.S. and Sc.D. degrees from Columbia University, New York, in 1997 and 1999. From 1997 to 2000 he was with Texas Instruments in Warren, New Jersey, working on high-speed filters and data converters, and from 2000 to 2002 with Bigbear Networks in Sunnyvale, California, on high-speed adaptive equalization for optical links. He joined IIT Madras in 2002, where he is now the NT Alexander Institute Chair Professor of Electrical Engineering and Dean (Academic Research). He has held visiting positions at Fairchild Semiconductor and with the High Speed Converters Group at Analog Devices, Toronto. His research interests are in high-speed analog circuit design, data converters and signal processing. Much of his recent work concerns continuous-time pipelined (CTP) ADCs – wideband converters combining high dynamic range with inherent anti-alias filtering – alongside continuous-time delta-sigma modulators and integrated filters. He is a co-author of Circuit Analysis for Analog, Mixed-Signal and RF Designers (with G. C. Temes, Wiley-IEEE Press, 2026); Understanding Delta-Sigma Data Converters, 2nd edition (with R. Schreier and G. C. Temes, Wiley-IEEE Press, 2017), which received the Wiley-IEEE Press Professional Book Award in 2020; and High Frequency Continuous Time Filters in Digital CMOS Processes (with Y. Tsividis, Kluwer, 2000). He is a Fellow of the IEEE, the Indian National Academy of Engineering and the Indian National Science Academy. His awards include the Shanti Swarup Bhatnagar Prize (2012), the Swarnajayanti Fellowship (2009), the IEEE Circuits and Systems Society Darlington Best Paper Award (2009) and the J. C. Bose Research Grant (2025). He was Editor-in-Chief of the IEEE Transactions on Circuits and Systems I (2014–15), and Vice President, Publications, of the IEEE Solid-State Circuits Society (2021–23). He has been an Associate Editor of the IEEE Journal of Solid-State Circuits, a member of the ISSCC technical programme committee, and a Distinguished Lecturer of the Solid-State Circuits and Circuits and Systems Societies.

References and Notes:

- S. Pavan, S. Manivannan and N. Basavaraj, “Analysis and design of wideband filtering ADCs using continuous-time pipelining,” IEEE J. Solid-State Circuits, 2024.
- S. Pavan, “Fundamentals of continuous-time ADCs – Part one: the continuous-time pipeline,” IEEE Solid-State Circuits Mag., vol. 16, no. 3, pp. 45–54, 2024.
- C. Kumar and S. Pavan, “Weak nonlinearities in active filters and continuous-time pipeline ADCs,” IEEE Trans. Circuits Syst. I, vol. 72, no. 12, pp. 7565–7577, 2025.
- N. Basavaraj, N. Rao, J. Seetharaman and S. Pavan, “Continuous-time pipelined ADC with background reconstruction-filter tracking,” IEEE Trans. Circuits Syst. I, 2026.



Wideband Filtering Analog-to-Digital Converters using Continuous-Time Pipelining

Dr. Shanthi Pavan*

*Department of Electrical Engineering
Indian Institute of Technology Madras
(e-Mail: shanthi@ee.iitm.ac.in)*

Wideband data converters are central to modern RF receivers, software-defined radio, and multi-GHz communication systems, where achieving high resolution over large signal bandwidths remains a fundamental challenge. This talk presents continuous-time pipelined (CTP) ADCs as a route to wideband, high-dynamic-range conversion, examining how distributing quantization across cascaded continuous-time stages relaxes the speed and linearity demands placed on any single stage while preserving inherent filtering of out-of-band interferers and noise. It turns out that a CT-pipeline ADC is a fundamental improvement over a conventional signal chain consisting of an anti-alias filter followed by an ADC. These concepts are illustrated through recent IC implementations at IIT Madras.

References and Notes:

1. Pavan, S.; Manivannan, S.; Basavaraj, N. IEEE Journal of Solid-State Circuits 2024.
2. Pavan, S. IEEE Solid-State Circuits Magazine 2024, 16, page 45 - page 54.
3. Pavan, S.; Shibata, H. IEEE Transactions on Circuits and Systems II: Express Briefs 2021, 68, page 810 - page 815.
4. Basavaraj, N.; Pavan, S. IEEE Transactions on Circuits and Systems I: Regular Papers 2023, 70, page 5086 - page 5097.
5. Manivannan, S.; Pavan, S. IEEE Solid-State Circuits Letters 2021, 4, page 92 - page 95.
6. Kumar, C.; Pavan, S. IEEE Transactions on Circuits and Systems I: Regular Papers 2025, 72, page 7565 - page 7577.
7. Basavaraj, N.; Rao, N.; Seetharaman, J.; Pavan, S. IEEE Transactions on Circuits and Systems I: Regular Papers 2026.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

M. Durga PRAKASH

Associate Professor

Department of Electronics and Communication Engineering
SRM University-AP, Amaravati, Andhra Pradesh

e-Mail: durgaprakash.m@srmap.edu.in

Homepage: <https://www.srmap.edu.in/faculty/dr-durga-prakash-m/>



Dr. M. Durga Prakash is currently Associate Professor at Department of Electronics and Communication Engineering, SRM University-AP in Andhra Pradesh. Dr. Prakash graduated in 2015 from Indian Institute of Technology Hyderabad with a Doctor of Philosophy (Ph.D) in the area of Microelectronics and VLSI in the Department of Electrical Engineering. His M.Tech (Bio-medical Engineering) 2009 and B.Tech (Electronics and Instrumentation Engineering) 2005 degrees are First Class with Distinction. He successfully completed two research projects funded by the DST-SERB, Government of India, outlay more than 50 lakhs. He has over 80+ research papers in prominent international journals and fully refereed international conferences and has 15 years of expertise. He also filed and published six patents. Prakash has supervised Six Ph.D. students and Five PhD students are currently undergoing on his guidance, and he has guided 30 M.Tech students. The key research fields are Micro/Nano electronics, Semiconductor Technology, Biosensors, VLSI circuits, and MEMS/NEMS. Dr. Durga Prakash is a Senior member in IEEE Member, Fellow in IETE and Life member in ISTE, MRSI.



From Advanced Semiconductor Devices to Energy-Efficient Integrated Circuits

M. Durga Prakash

Department of Electronics and Communication Engineering

SRM University-AP, Amaravati

(e-Mail: durgaprakash.m@srmmap.edu.in)

The continuous scaling of semiconductor technology demands innovative device architectures and circuit-design approaches to achieve high performance, low power consumption, and enhanced functionality. This workshop focuses on the integration of advanced semiconductor devices and emerging electronic materials with modern chip-design methodologies. The research work explores nanoscale transistor architectures, including FinFETs, Gate-All-Around (GAA) FETs, and Carbon Nanotube Field-Effect Transistors (CNTFETs), with emphasis on their electrical characteristics, switching performance, power consumption, and suitability for next-generation integrated circuits. The influence of novel dielectric and semiconductor materials on device performance is also investigated to address the challenges associated with continued device scaling. Device-level analysis and modelling are further extended toward circuit-level implementation, including logic gates, low-power digital circuits, and sensor-interface applications. The workshop provides an opportunity to understand the complete design perspective, from semiconductor material and device engineering to transistor-level and system-oriented chip design. The outcomes highlight the potential of advanced device architectures and emerging materials for developing energy-efficient, high-performance, and application-specific integrated circuits for future electronic systems.

Keywords:

Chip Design, Semiconductor Devices, FinFET, GAA FET, CNTFET, Emerging Materials, Low-Power VLSI, Integrated Circuits.

References and Notes:

1. Scognamiglio, Luca, Fabrizio Mo, Chiara Elfi Spano, Marco Vacca, and Gianluca Piccinini. "Simulation study on the impact of miniaturization in 3 nm node 3D junctionless transistors." *IEEE Transactions on Nanotechnology* 24 (2025): 102-109.
2. Choi, JinYoung, HyunJoon Jeong, Yohan Kim, Sajjan Parajuli, Sagar Shrestha, Gyoujin Cho, Jeong-Taek Kong, and SoYoung Kim. "A neural-network-based statistical compact model using a variational autoencoder for emerging transistors." *IEEE Transactions on Electron Devices* 72, no. 7 (2025): 3364-3370.
3. Rossoni, Angelo, Tomasz Brozek, Sharad Saxena, Rajesh Khamankar, Luigi Colalongo, and Zsolt M. Kovacs-Vajna. "Stress-related local layout effects in FinFET technology and device design sensitivity." *IEEE Transactions on Semiconductor Manufacturing* 38, no. 2 (2025): 117-125.
4. Sarkar, Eknath, Chengyang Zhang, Dyutimoy Chakraborty, Sharadindu Gopal Kirtania, Khandker Akif Aabrar, Hyeonwoo Park, Jaewon Shin et al. "First demonstration of high-performance and extremely stable W-doped In₂O₃ gate-all-around (GAA) nanosheet FET." *IEEE Transactions on Electron Devices* 72, no. 5 (2025): 2662-2666



Viveka, KONANDUR RAJANNA
Assistant Professor

Department of Electronic Systems Engineering (ESE)
Indian Institute of Science (IISc)

e-Mail: krviveka@IISc.ac.in

Homepage: <https://labs.dese.iisc.ac.in/viveka/>



Dr. Viveka Konandur Rajanna is an Assistant Professor in the Department of Electronic Systems Engineering (ESE) at the Indian Institute of Science (IISc), Bengaluru. His research focuses on energy-efficient VLSI systems for artificial intelligence and edge computing, spanning AI accelerators, in-memory computing, low-power memories, approximate computing, hardware security, and human-machine interfaces.

He received his M.Tech. and Ph.D. degrees from IISc and subsequently conducted research at the National University of Singapore and the Berkeley Education Alliance for Research in Singapore before joining IISc in 2022. Prior to his academic career, he worked as a Design Engineer at Analog Devices.

His research spans circuits, architectures, and hardware algorithm co-design, with multiple silicon demonstrations. His work has been published in leading solid-state circuits and VLSI venues, including JSSC, ISSCC, VLSI Symposium, CICC, and ESSCIRC.

Representative Publications:

- [1] T. Wang, J. Basu, V. K. Rajanna, and M. Alioto, "SRAM Static Entropy Extraction From Every Single Transistor in Unmodified Bitcell and Data Fingerprinting for Provenance Assurance," IEEE JSSC, vol. 61, no. 2, pp. 690–703, 2026.
- [2] A. Gupta, J. Vohra, V. K. Rajanna, and M. Alioto, "122.7 TOPS/W Stdcell-Based DNN Accelerator Based on Transition Density Data Representation, Clock-Less MAC Operation, Pseudo-Sparsity Exploitation in 40 nm," IEEE VLSI Symp., pp. 1–2, 2024.
- [3] A. Gupta, V. K. Rajanna, T. Singh, S. Jain, O. Aiello, P. Crovetto, and M. Alioto, "DDPMnet: All-Digital Pulse Density-Based DNN Architecture With 228 Gate Equivalents/MAC Unit, 28 TOPS/W and 1.5 TOPS/mm² in 40 nm," IEEE CICC, pp. 1–2, 2022.
- [4] S. Taneja, V. K. Rajanna, and M. Alioto, "Unified In-Memory Dynamic TRNG and Multi-Bit Static PUF Entropy Generation for Ubiquitous Hardware Security," IEEE JSSC, vol. 57, no. 1, pp. 153–166, 2022; also presented at IEEE ISSCC, pp. 498–500, 2021.
- [5] V. K. Rajanna and M. Alioto, "On-Chip Links With Energy-Quality Tradeoff in Error-Resilient and Machine Learning Applications," IEEE JSSC, vol. 56, no. 11, pp. 3533–3543, 2021.
- [6] V. K. Rajanna, S. Taneja, and M. Alioto, "SRAM With In-Memory Inference and 90% Bitline Activity Reduction for Always-On Sensing With 109 TOPS/mm² and 749–1,459 TOPS/W in 28 nm," IEEE ESSCIRC, pp. 127–130, 2021.
- [7] P. Agarwal, V. K. Rajanna, T. W. Da, B. C. K. Tee, and M. Alioto, "Fully-Digital Self-Calibrating Decoder With Sub- μ W, 1.6 fJ/conv-step and 0.0075 mm² per Receptor for Scaling to Human-Like Tactile Sensing Density," IEEE VLSI Symp., pp. 1–2, 2021.
- [8] V. K. Rajanna and M. Alioto, "Low-Swing Links With Dynamic Energy-Quality Trade-off for Error-Resilient Applications," IEEE CICC, pp. 1–4, 2019.
- [9] P. K. VS, L. S. Burle, S. N, and V. K. Rajanna, "Approximate DCT Using Scaling Factor Optimization for Error-Resilient Applications," IEEE ISCAS, 2026.



Intelligence at the Edge: Designing AI Within the Energy Budget

Dr. Viveka Konandur Rajanna
Department of Electronic Systems Engineering (ESE)
Indian Institute of Science (IISc)
(e-Mail: krviveka@IISc.ac.in)

Artificial intelligence is rapidly moving from the cloud to the edge, enabling intelligent capabilities in smartphones, wearables, autonomous systems, medical devices, and billions of connected sensors. However, bringing increasingly sophisticated AI models to these platforms presents a fundamental challenge: delivering greater intelligence within stringent energy, memory, computation, and thermal constraints. This talk examines Edge AI from a VLSI and hardware design perspective, focusing on the central question of how to achieve useful AI computation within a limited energy budget. It explores the growing importance of data movement and memory access in determining system efficiency and introduces key approaches including quantization, sparsity, specialized accelerator architectures, distributed memory, near sensor computing, and compute in memory. Through representative research examples, the talk illustrates how algorithm, architecture, memory, and circuit-level innovations can work together to improve energy efficiency. It concludes by highlighting emerging research opportunities in designing the next generation of intelligent edge systems.

References and Notes:

1. Horowitz, M. *IEEE International Solid-State Circuits Conference Digest of Technical Papers* 2014, 10–14.
2. Sze, V.; Chen, Y. H.; Yang, T. J.; Emer, J. S. *Proceedings of the IEEE* 2017, 105, 2295–2329.
3. Chen, Y. H.; Krishna, T.; Emer, J. S.; Sze, V. *IEEE Journal of Solid-State Circuits* 2017, 52, 127–138.
4. VS, P. K.; Burle, L. S.; N, S.; Rajanna, V. K. *IEEE International Symposium on Circuits and Systems (ISCAS)* 2026.
5. Taneja, S.; Rajanna, V. K.; Alioto, M. *IEEE Journal of Solid-State Circuits* 2022, 57, 153–166.
6. Rajanna, V. K.; Alioto, M. *IEEE Journal of Solid-State Circuits* 2021, 56, 3533–3543.
7. Rajanna, V. K.; Taneja, S.; Alioto, M. *IEEE European Solid State Circuits Conference (ESSCIRC)* 2021, 127–130.
8. Agarwal, P.; Rajanna, V. K.; Da, T. W.; Tee, B. C. K.; Alioto, M. *Symposium on VLSI Circuits* 2021, 1–2.
9. Rajanna, V. K.; Amrutur, B. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 2016, 24, 1663–1674.



S RAMPRASATH

Assistant Professor

Department of Electrical Engineering
Indian Institute of Technology Madras

e-Mail: ramprasath@ee.iitm.ac.in

Homepage: <https://home.iitm.ac.in/ramprasath/>



S. Ramprasath is an Assistant Professor in the Department of Electrical Engineering at IIT Madras, where he works on Electronic Design Automation (EDA), with a focus on analog/mixed-signal layout automation and combinatorial optimization using Ising machines. He received his Ph.D. in Electrical Engineering (Microelectronics and VLSI) from IIT Madras in 2016 and his B.Tech. in Electronics and Communication Engineering from NIT Tiruchirappalli in 2009. Before joining IIT Madras, he was a Postdoctoral Associate at the University of Minnesota, Twin Cities, under Prof. Sachin S. Sapatnekar, where he was a primary contributor to ALIGN, an open-source SPICE-to-GDSII analog layout generator. He has also held industry roles at Synopsys (Galaxy Custom Router) and holds a U.S. patent on keep-through regions for end-of-line routing rules.

References and Notes:

- [1] S. Ramprasath, A. K. Sharma, M. Madhusudan, S. Yaldiz, J. Poojary, R. Harjani, S. M. Burns, and S. S. Sapatnekar, "Analog/Mixed-Signal Layout Optimization using Optimal Well Taps," *Proc. ACM International Symposium on Physical Design (ISPD)*, 2022.
- [2] T. Dhar, S. Ramprasath, J. Poojary, S. Yaldiz, S. Burns, R. Harjani, and S. S. Sapatnekar, "A Charge Flow Formulation for Guiding Analog/Mixed-Signal Placement," *Proc. Design, Automation and Test in Europe (DATE)*, 2022.
- [3] S. Ghosh, S. S. Peri, S. Ramprasath, S. A. Berhan, E. Y. Gebru, R. Harjani, and S. S. Sapatnekar, "COMPOSER: Circuit Optimization of mm-Wave/RF Circuits with Performance-Oriented Synthesis for Efficient Realizations," *Proc. ACM/IEEE Design Automation Conference (DAC)*, 2026.



Automatic Analog/Mixed-Signal Layout Synthesis Using Open-Source Tools

Dr. S Ramprasath

Department of Electrical Engineering

Indian Institute of Technology Madras

(e-Mail: ramprasath@ee.iitm.ac.in)

Analog, mixed-signal, and RF (AMS/RF) layout remains stubbornly manual even as digital layout has been fully automated, because prior automation approaches fail to give designers fine-grained control. Academic tools such as BAG, ALIGN, MAGICAL, and FASoC are each silicon-proven but fall short in practice: BAG demands generator scripting, ALIGN suffers long runtimes and format friction with commercial flows, MAGICAL inherits ALIGN's issues plus a difficult per-technology design-rule abstraction, and FASoC's reuse of digital P&R tools leaves it unable to handle symmetry, common-centroid, and alignment constraints. Drawing on experience authoring ALIGN's placer and router [1], this talk presents a new *assisted-automation* flow that keeps the designer's intent and constraints central rather than replacing them, built around an in-house analytical placer and the Hanan Grid Router [2]: a rectilinear A*-based detail router supporting mirror-symmetric net routing, SAT-verified pin escape, and multi-threaded routing, interoperable with ALIGN's JSON/LEF formats. The approach has already shown a significant layout-time reduction on a 4-antenna MIMO RX case study relative to manual layout, and is now being validated on two new circuit classes: a Wi-Fi/Bluetooth-band RF receiver and a DAC, taped out in TSMC 65nm early this year and are awaiting testing to Silicon-prove the technique. The whole flow is also being ported to the KLayout editor [3].

References and Notes:

1. K. Kunal et al., "Reinforcing the Connection between Analog Design and EDA," ASP-DAC, 2024; ALIGN open-source project, github.com/ALIGN-analoglayout/ALIGN-public.
2. Hanan Grid Router, github.com/srini229/hanan_router.
3. KLayout, <https://klayout.de/>



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Justin, ROMSTADT

Postdoctoral Researcher

Group Leader, RF Systems and Circuits

Institute for CMOS Design

Technical University Braunschweig

e-Mail: j.romstadt@tu-braunschweig.de

Homepage: [linkedin.com/in/justin-romstadt-521282114](https://www.linkedin.com/in/justin-romstadt-521282114)



Justin Romstadt received the B.Sc. and M.Sc. degrees in electrical engineering from Ruhr University Bochum, Germany, in 2016 and 2019, respectively, and the Ph.D. degree with highest distinction in 2025.

From 2019 to 2026, he was a Research Assistant with the Institute of Integrated Systems at Ruhr University Bochum. His research focused on high-frequency measurement systems based on SiGe MMICs, integrated D-band radar circuits, and the development of D-band VNA extension modules. Since 2026, he has been with the Institute for CMOS Design at TU Braunschweig, where he leads the RF Systems and Circuits Research Group.

His research interests include millimeter-wave and sub-terahertz integrated circuits and systems, high-frequency measurement techniques, and radar systems. He serves as a reviewer for the IEEE Journal of Solid-State Circuits, IEEE Microwave and Wireless Technology Letters, and IEEE Transactions on Terahertz Science and Technology. He is a co-organizer of “Junges Forum” for German Microwave Conference 2027 (GeMiC) and was a co-recipient of the Second Place Award in the Student Paper Competition at IEEE RWW 2025.

Representative publications:

J. Romstadt et al., “[Proving the Feasibility of D-Band Single SiGe MMIC Vector Network Analyzer Extension Modules With Large System Dynamic Range](#),” IEEE Journal of Microwaves, 2024.

J. Romstadt et al., “[A 117.5–155-GHz SiGe \$\times 12\$ Frequency Multiplier Chain With Push-Push Doublers and a Gilbert Cell-Based Tripler](#),” IEEE Journal of Solid-State Circuits, 2023.

H. Papurcu, J. Romstadt et al., “[A Wideband Four-Channel SiGe D-Band Transceiver MMIC for TDM MIMO FMCW Radar](#),” IEEE 23rd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2023.



Millimeter-Wave Integrated Circuit Research at the Institute for CMOS Design: Current Activities and Perspectives toward 140 GHz PMCW Radar

Dr. Justin Romstadt
Institute for CMOS Design
TU Braunschweig
(e-Mail: j.romstadt@tu-braunschweig.de)

This talk starts with a brief overview of the Institute for CMOS Design at TU Braunschweig and its research in analog, RF and millimeter-wave, and cryogenic integrated circuits. One focus of these activities is the development of highly integrated radar systems. The presentation then turns to automotive in-cabin sensing, where millimeter-wave radar is becoming increasingly relevant for applications such as occupant detection, child-presence detection, and vital-sign monitoring. This demand motivates the exploration of newly emerging spectrum for in-cabin radar between 122 and 148.5 GHz, comprising two separate frequency ranges. Within this context, the talk introduces the concept of a highly integrated PMCW radar operating in the upper frequency range around 140 GHz. The architecture combines continuous transmission, pseudo-random phase modulation, and correlation in the receiver. Emphasis is placed on individual components, such as the amplifiers or the IQ correlator as a central element of the system, and on the architectural challenges associated with the implementation.

References and Notes:

1. V. Lasserre et al., "A 5.6 dB NF Two-Stage 110 - 125 GHz LNA Gain-Boosted by RC-over-Neutralization for Radar Applications in 28 nm CMOS," 2024 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Fort Lauderdale, FL, USA, 2024, pp. 146-149.
2. S. Koop-Brinkmann, V. Lasserre and V. Issakov, "A Calibration-Free 55-to-70 dBc H1 Rejection, 13.8 % Efficiency, 102-to-120 GHz CMOS Frequency Tripler using Phase-Alignment Technique for Harmonic Recombination," 2026 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2026, pp. 275-278.
3. R. Zhou et al., "A 25% PAE 14 dBm Harmonic-Shaping 110 GHz Power Amplifier using modified EMCC as Power Combiners in 22 nm FDSOI CMOS," IEEE ESSERC 2026, tbp.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Andrew Roobert A
Assistant Professor

Department of ECE
SRM Institute of Science and Technology, Kattankulathur

e-Mail: andrewra@srmist.edu.in

Homepage: <https://www.srmist.edu.in/faculty/dr-a-andrew-roobert/>



Dr. A. Andrew Roobert is an Assistant Professor in the Department of Electronics and Communication Engineering, College of Engineering and Technology, SRM Institute of Science and Technology. He holds a Ph.D. in Integrated Circuit Design from Thiagarajar College of Engineering, Madurai under Anna University Chennai, with a thesis focused on the design, analysis, and optimization of CMOS low-noise amplifiers for wireless applications. He has also completed a postdoctoral fellowship in Analog IC Design at IIT Guwahati, where his research involved PLLs, delay-cell and LC oscillators, active inductors, and mixed-signal circuit modeling. His research interests include analog and mixed-signal IC design, RF and wireless ICs, LNAs, PLLs, VCOs, low-power VLSI, circuit optimization, and analog front-end design. He has published research articles in peer-reviewed journals and has experience with commercial and open-source EDA tools for IC design, simulation, and implementation.

Relevant Publications:

1. "Design and analysis of 28 GHz CMOS low power LNA with 6.4 dB gain variability for 5G applications", Transactions on Emerging Telecommunications Technologies
2. "Design and analysis of a sleep and wake-up CMOS low noise amplifier for 5G applications" in Telecommunication Systems, Springer
3. "Design and Analysis of 0.9 GHz and 2.3 GHz Concurrent Dual-Band CMOS LNA for Mobile Communication" in International Journal of Circuit Theory and Applications, Wiley
4. "Design and Optimization of Feed Forward Noise Cancelling CMOS LNA for 2.4 GHz WLAN Applications" in IET Circuits, Devices and Systems
5. "Survey on parameter optimization of mobile communication band low noise amplifier design" in International Journal of RF and Microwave Computer-Aided Engineering, Wiley



CMOS Low-Noise Amplifier Design: Challenges, Trade-offs and Emerging Trends

Dr. A. Andrew Roobert*

Department of Electronics and Communication Engineering
SRM Institute of Science and Technology, Kattankulathur
(e-Mail: andrewra@srmist.edu.in)

Low-noise amplifiers (LNAs) are critical building blocks in RF receivers, where the performance of the first amplification stage has a significant influence on the overall receiver sensitivity. CMOS LNA design involves several competing requirements, including low noise figure, high gain, good linearity, wide bandwidth, impedance matching, stability, and low power consumption [1], [2]. This work presents the fundamental design considerations of CMOS LNAs and examines the trade-offs among these key performance parameters. Different LNA architectures and their suitability for various RF applications are discussed, with emphasis on device sizing, biasing, input matching, and parasitic effects [2], [3]. Optimization techniques are considered to identify suitable design parameters for achieving an appropriate balance among noise figure, gain, linearity, bandwidth, and power consumption [2]–[4]. Recent LNA implementations demonstrate the use of noise-cancellation, transformer-based matching, capacitive neutralization, and variable-gain techniques to address these trade-offs in advanced CMOS technologies [3]–[5]. Simulation-based performance evaluation using RF parameters such as S-parameters, noise figure, gain, and linearity is also considered. The discussion highlights how systematic optimization can improve LNA performance and enable robust designs for low-power, wideband, and advanced CMOS RF applications [2]–[5].

References and Notes:

1. B. Razavi, *RF Microelectronics*, 2nd ed., Prentice Hall, 2012.
2. Mohammad Zaid; Purnima Kumari; Ahtisham Pampori; Mohammad Sajid Nazir; Umakant Goyal; Meena Mishra, 'Optimizing Low Noise Amplifiers: A Two-Stage Approach for Improved Noise Figure and Stability', *IEEE Access*, vol. 12, pp. 53475–53484, Apr. 2024
3. Zhixian Deng; Jie Zhou; Huizhen Jenny Qian; Xun Luo, 'A 22.9–38.2-GHz Dual-Path Noise-Canceling LNA With 2.65–4.62-dB NF in 28-nm CMOS', *IEEE Journal of Solid-State Circuits*, Volume: 56, Issue: 11, November 2021
4. Chae Jun Lee; Hyohyun Nam; Dongki Kim; Seong-Kyun Kim; Dae Young Lee, 'A D-Band Variable Gain Low Noise Amplifier in a 28-nm CMOS Process for 6G Wireless Communications', *IEEE Transactions on Circuits and Systems II: Express Briefs*, Volume: 71, Issue: 1, January 2024
5. Jian Hua Jiang; Li Gao; Xiu Yin Zhang, 'A 0.5–44-GHz LNA With 23-dB Peak Gain and 3-dB Average NF in 28-nm CMOS Technology', *IEEE Transactions on Microwave Theory and Techniques*, vol. 73, no. 12, pp. 10855–10864, Dec. 2025.



Prateek Kumar SHARMA

Assistant Professor

Department of Electrical Engineering
Indian Institute of Technology Tirupati

e-Mail: prateek.sharma@iittp.ac.in

Homepage: <https://facweb.iittp.ac.in/~prateek.sharma/about.html>



Dr. Prateek Kumar Sharma received his M.S. and Ph.D. degrees in Electrical Engineering from the Indian Institute of Technology Guwahati, India, in 2017 and 2021, respectively. During his doctoral studies, he focused on RF front-end modules for full-duplex and MIMO 5G receivers. In 2020, he joined the GlobalFoundries IP design team in Bangalore, where he worked on high-speed analog transceivers for silicon photonics across various GF technologies. In 2024, he worked on the Intel Foundry Services team in Bangalore. He has previous experience with advanced FinFET technologies in RF/mm-wave and analog circuits.

His research interests include RF/mm front-end modules, high-speed analog circuits for silicon photonics, and terahertz circuits for communications. Prateek was a recipient of the National Meritorious Invention Award of the Year 2019 from the Government of India. He was also a finalist for the Best Student Paper at the IEEE RFIC 2021 conference and received the VLSID Best Poster Award in 2020 for his work titled “New Generation of RF Circuits for 5G NR” in the Student Research Forum category.

Research Areas

RF/mm-wave front-end modules for full-duplex and MIMO transceivers, High-speed analog mixed signal circuits for wireline applications, 3D Heterogeneous integration for silicon photonics and RFICs, High ft/fmax CMOS, SiGe, and GaN technologies for D-band applications.

Representative publications

1. P. K. Sharma and N. Nallam, “Breaking the Performance Tradeoffs in N-Path Mixer-First Receivers Using a Second- Order Baseband Noise-Canceling TIA,” in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 11, pp. 3009-3023, Nov. 2020.
2. P. K. Sharma and N. Nallam, “A 0.1–0.95 GHz Full-Duplex Receiver With < 1 dB NF Degradation Using a Passive Continuous-Mode Charge-Sharing Vector Modulator,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 3042-3052, July 2019.



Complementary SiGe RF Front-End Circuits for FR3 and mm-Wave Applications

Dr. Prateek Kumar Sharma
Department of Electrical Engineering
Indian Institute of Technology Tirupati
(e-Mail: prateek.sharma@iittp.ac.in)

A 130-nm SiGe BiCMOS technology from GlobalFoundries offers high-speed complementary HBTs, with PNP devices achieving (f_T/f_{max}) of 210/240 GHz and NPN devices reaching 420/430 GHz. While NPN HBTs are traditionally preferred for high-frequency RF circuits, the high-speed PNP device offers additional design freedom, analogous to the complementary NMOS/PMOS devices available in CMOS technologies. This talk explores the use of complementary SiGe HBTs for RF front-end circuits targeting FR3 and mm-wave applications. We present broadband, cascode-less LNAs that employ frequency-selective gain enhancement via complementary SiGe devices. The proposed LNA combines a neutralized NPN differential pair with a cross-coupled PNP auxiliary stage to enhance the effective transconductance while maintaining unconditional stability over a wide frequency range. The complementary PNP device enables additional flexibility in gain enhancement without significantly increasing the supply voltage. We further discuss the design and operation of a Class-E power amplifier employing complementary SiGe HBTs, highlighting the potential of PNP devices for efficient power generation.

References and Notes:

1. **P. K. Sharma**, V. Ruparelia, S. Sirohi, U. S. Raghunathan, V. Vanukuru, and V. Jain. “Design Trade-offs between Series-Peaking Inductor and High f_T SiGe HBTs in Transimpedance Amplifiers.” 2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Monterey, CA, USA, pp. 167–170.
2. Vibhor Jain, John Pekarik, Crystal Kenney, Judson Holt, Chris Durcan, Jeffrey B. Johnson, Sudesh Saroop, Mona Nafari, Vaibhav Ruparelia, Santosh Kumar Gedela, **Prateek Kumar Sharma**, Viorel Ontalus, Shweta Khokale, Saloni Chaurasia, Venkata Vanukuru, Alvin Joseph. “415/610GHz f_T/f_{MAX} SiGe HBTs Integrated in a 45nm PDSOI BiCMOS Process.” 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, pp. 11.6.1–11.6.4.
3. Uppili S. Raghunathan, Saurabh Sirohi, Vaibhav Ruparelia, **Prateek Kumar Sharma**, Dimitris P. Ioannou, Vibhor Jain, H.K. Kakara, S. Gedela, Venkat Vanukuru, P. Dongmo, C. Luce, R. Hazbun, R. Krishnasamy, J. Hwang, M. Levy, Kristin Welch, S. Liu, B. Cucci, S. Cole, J. Kantarovsky, A. Vallett, I. McCallum-Cook, M. Yu, R. Phelps, A. Divergilio, A. Sturm, M. Peters, S. Johnson, R. Rassel, M. Lagerquist, M. Kerbaugh, K. Newton, J. Pekarik, Q. Liu. “Performance Improvements of SiGe HBTs in 90nm BiCMOS Process with f_T/f_{max} of 340/410 GHz.” 2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Phoenix, AZ, USA, pp. 232–235.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Rahul SINGH

Assistant Professor

Department of Electrical Engineering
IIT Bombay, India

e-Mail: rahuls@ee.iitb.ac.in

Homepage: <https://rahuls-ee.github.io/hfic/>



Rahul Singh received the B.Tech degree in Electronics Engineering from Indian Institute of Technology (BHU), Varanasi, India, in 2008, and the M.S. degree from Seoul National University, Seoul, South Korea, in 2011, and the Ph.D degree from Carnegie Mellon University, PA, USA in 2018. From 2011 to 2013, he was with the Processor Development Group, Samsung Electronics, South Korea. From 2018 to January 2024, he was with Qualcomm Inc., San Diego, CA, USA, where I worked on the development of integrated radio-frequency (RF) transceivers for cellular and base-station applications. He is a Senior Member of IEEE. His research interests are broadly on the design and development of analog/RF/millimeter-wave (mm-wave) integrated circuits, systems and architectures for current and emerging communication technologies, including highly integrated multi-mode transceivers for sub-6 GHz and the development of multi-element beamforming transceivers for emerging 6G applications. He is also interested in developing circuit and system-level digital/mixed-signal calibration techniques for robust RF transceivers resilient to analog imperfections.

Representative Publications:

1. M Lakshmi Deep Chowdary, L. Somappa, and R. Singh, “A Perturbation-Based Low-Overhead IQ Calibration Scheme for RF Receivers,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Shanghai, China, pp. 1462-1466, 2026. ([link](#))
2. R. Singh, S. Mondal and J. Paramesh, “A Millimeter-wave Receiver Using a Wideband Low-Noise Amplifier with One-Port Coupled Resonator Loads,” *IEEE Trans. on Microwave Theory and Techniques*, vol. 68, no. 9, pp. 3794-3803, Sept. 2020. ([link](#))
3. R. Singh, S. Mondal and J. Paramesh, “A Compact Digitally-Assisted Merged LNA Vector Modulator Using Coupled Resonators for Integrated Beamforming Transceivers,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 2555-2568, Jul. 2019. ([link](#))
4. S. Mondal, R. Singh, A. I. Hussein, and J. Paramesh, “A 25-30 GHz Fully-Connected Hybrid Beamforming Receiver for MIMO Communication,” *IEEE Journal of Solid-State Circuits*, vol. 53, pp. 1275-1287, May 2018. ([link](#))



A Low-Overhead, Perturbation-Based Approach for Fast, Lean and Accurate RF IQ Calibration

Dr. Rahul Singh

Department of Electrical Engineering
Indian Institute of Technology Bombay
(e-Mail: rahuls@ee.iitb.ac.in)

In-phase and quadrature (IQ) imbalance is a fundamental impairment in direct-conversion receiver architectures, limiting image rejection ratio (IRR) and signal-to-noise (SNR) critical for higher order modulation schemes. While digital-domain IQ calibration techniques are well-established, conventional approaches can incur prohibitive hardware overhead, complex matrix inversions, or high computational latency—making them ill-suited for power-constrained, high-throughput, or multi-antenna RF front-ends. This talk revisits the classic IQ calibration challenge through the lens of hardware-efficient digital assistance. Based on our recent work published at ISCAS 2026*, we present a perturbation-based IQ calibration scheme that drastically reduces both circuit footprint and digital processing complexity. By introducing a controlled, low-complexity perturbation mechanism into the receiver path, the scheme enables rapid parameter extraction and correction without requiring high-bit-width multipliers, or extensive memory buffers. We will cover the theoretical formulation, hardware implementation, and key performance metrics—demonstrating significant IRR recovery with minimal area and power overhead. While this approach is restricted to a single-tone/narrowband calibration, we will discuss how this framework can be generalized to wideband architectures.

References and Notes:

1. M Lakshmi Deep Chowdary, L. Somappa, and R. Singh, “A Perturbation-Based Low-Overhead IQ Calibration Scheme for RF Receivers,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Shanghai, China, pp. 1462-1466, 2026.



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Laxmeesha SOMAPPA

Assistant Professor

Department of Electrical Engineering
IIT Bombay, Mumbai

e-Mail: laxmeesha@ee.iitb.ac.in

Homepage: <https://homepages.iitb.ac.in/~laxmeesha/>



Laxmeesha Somappa is an Assistant Professor in the Department of Electrical Engineering at the Indian Institute of Technology Bombay (IIT Bombay), India. Prior to joining IIT Bombay, he was a postdoctoral researcher in the Integrated Neurotechnologies Laboratory at École Polytechnique Fédérale de Lausanne (EPFL), Switzerland, affiliated with the Center for Neuroprosthetics (Neuro-X Institute) at Campus Biotech, Geneva. He has also served as a visiting researcher at the Nanoscience Centre at the University of Cambridge, UK. Dr. Somappa received his M.Tech. in Microelectronics and VLSI from IIT Madras in 2015 and his Ph.D. from IIT Bombay in 2021, focusing on multi-channel biomedical delta-sigma data converters. Between 2011 and 2013, he held industry engineering roles at Tata Elxsi and Qualcomm India.

His research interests center on integrated analog, digital, and mixed-signal circuits and systems for biomedical instrumentation and precision sensor interfaces. His current work emphasizes energy-efficient closed-loop neuromodulation SoCs with on-chip ML integration, ultra-low-power analog front end and data converters, high-voltage circuits for implantable stimulators, FPGA-based mixed-signal SoC testing, and hardware-algorithmic co-design for reconfigurable sensor networks.



Closed-Loop Neuromodulation SoCs for Neurological Disorders

Laxmeesha Somappa
Department of Electrical Engineering
Indian Institute of Technology Bombay
(e-Mail: laxmeesha@ee.iitb.ac.in)

Based on worldwide estimations, 60–70 million people annually suffer from traumatic injuries to the nervous system. These injuries impose severe neural disorders, long-term disabilities, and substantial lifetime costs on patients. Neuromodulation can alleviate disease symptoms and restore lost neurological function by delivering targeted electrical therapies. Recently, energy- and area-efficient implantable closed-loop neuromodulation system-on-chips (SoCs) have emerged to significantly enhance therapeutic efficacy while minimizing side effects compared to traditional open-loop approaches. This talk will discuss state-of-the-art SoC architectures designed for responsive epileptic seizure suppression and adaptive deep brain stimulation (DBS) for Parkinson's disease [1, 2]. We will examine critical circuit- and system-level design challenges, including achieving sub-microwatt multi-channel biopotential acquisition, mitigating massive stimulation artifacts to prevent front-end saturation, and implementing ultra-low-power on-chip ML classifiers for real-time biomarker detection [3, 4, 5], on-chip security for open-loop high-voltage stimulators and their ESD protection, neural signal compression for open-loop recording [6]. Finally, the presentation will highlight silicon implementations and experimental validations, concluding with future perspectives on scaling channel density, edge intelligence, and reliability in next-generation therapeutic neural implants.

References and Notes:

1. U. Shin, et al., "A 256-Channel 0.227 μ J/class Versatile Brain Activity Classification and Closed-Loop Neuromodulation SoC with 0.004mm²-1.51 μ W/channel Fast-Settling Highly Multiplexed Mixed-Signal Front-End," 2022 IEEE International Solid-State Circuits Conference (ISSCC)
2. U. Shin, C. Ding, L. Somappa, V. Woods, A. S. Widge and M. Shoaran, "A 16-Channel 60 μ W Neural Synchrony Processor for Multi-Mode Phase-Locked Neurostimulation," 2022 IEEE Custom Integrated Circuits Conference (CICC)
3. A. P. Sharma, K. A. Rao and L. Somappa, "Hardware Optimization and Implementation of a 16-Channel Neural Tree Classifier for On-Chip Closed-Loop Neuromodulation," in IEEE Transactions on Biomedical Circuits and Systems, vol. 19, no. 2, pp. 244-256, April 2025
4. L. Iyer, A. Bal and L. Somappa, "Calibration-Enhanced 16-Channel On-Chip Seizure Classifier using Gated Recurrent Network," 2025 IEEE International Symposium on Circuits and Systems (ISCAS)
5. A. Gupta and L. Somappa, "A 16-Channel Rapid On-Chip Seizure Classifier with Online Re-Training for Closed-loop Neuromodulation," 2026 IEEE International Symposium on Circuits and Systems (ISCAS)
6. S. S. Baliyan, A. Thakur and L. Somappa, "On-chip Data Compression Techniques for High-Density Implantable Neural Recording," 2024 IEEE International Symposium on Circuits and Systems (ISCAS)



Early-Career Scientist Workshop on Chip Design 5 – 7 October 2026

Nils Hendrik, STANISLAWSKI
Research Associate

Institute of Microelectronic Systems
Leibniz University Hannover

e-Mail: nils.stanislawski@ims.uni-hannover.de

Homepage: <https://www.ims.uni-hannover.de/institut/personenverzeichnis/stanislawski>



Nils Stanislawski is a research associate at the Institute of Microelectronic Systems (IMS) at Leibniz University Hannover, Germany. His background spans embedded and microelectronic systems, hardware and software development, and laboratory automation.

His earlier work focused on automated systems for biomedical and laboratory applications, including bioreactor automation for tissue-engineered vascular grafts and technical contributions to early-response and diagnostic infrastructures during the COVID-19 pandemic. This work shaped his interest in reliable embedded systems, automation, and hardware–software integration for complex experimental environments.

His current work increasingly focuses on digital chip design and design enablement, including digital ASIC design, hardware security and IP protection, open-source EDA, FPGA prototyping, and accessible design-to-tape-out methodologies. A central goal is to lower barriers between academic concepts and practical semiconductor implementations.

Beyond his technical research, he leads activities on young talent and specialist development within the Chipdesign Germany network and contributes to the scientific accompanying research of the German Open Source DE:Sign projects. These activities focus on strengthening chip-design capabilities in Germany and Europe, accessible design infrastructures, and education pathways from school students to early-career researchers.

He also plays a leading role in the nationwide student competition Invent a Chip and initiated the International Summer School on Microelectronics (ISSOM), bringing together students, early-career researchers, academia, and industry from different countries.



Invent a Chip: Opening Microelectronics to Future Chip Designers

Nils Hendrik Stanislawski
Institute of Microelectronic Systems
Leibniz University Hannover
(e-Mail: nils.stanislawski@ims.uni-hannover.de)

Open-source EDA for digital designs has matured significantly in recent years. Today, open tools can cover large parts of the workflow from HDL entry and simulation to synthesis, place-and-route, FPGA implementation, and even ASIC tape-out. However, these tools are often developed for expert users and remain a fragmented landscape of editors, simulators, synthesis tools, hardware interfaces, and design flows, making them difficult to approach for pupils and students without prior experience. Initiatives such as Tiny Tapeout have demonstrated that parts of this process can be made accessible even to newcomers, although such approaches necessarily focus on a constrained workflow and design space rather than providing a general-purpose environment for learning and experimenting with digital design.

This presentation introduces our work around Germany's nationwide student competition *Invent a Chip* and the development of open-source solutions for hands-on education in digital chip design. The competition enables school students to progress from basic digital concepts toward practical hardware development. Building on these experiences, we are developing a freely accessible, open-source teaching platform that introduces the foundations of digital design and progressively leads learners toward HDLs and simulation. It is complemented by a development environment for practical design work, integrating HDL editing, simulation, visualization, synthesis, and interaction with FPGA hardware. Together, both tools are intended to support school-level education as well as university lectures and laboratory courses. The focus is on reducing setup complexity, providing reproducible workflows, and combining existing open-source tools into an approachable environment for learning modern digital-design methods. The presentation will discuss the educational motivation, current implementation approaches, and lessons learned from making these workflows accessible to future chip designers.

To place these educational efforts in a broader context, the presentation will also highlight other German initiatives that aim to make chip design more accessible and attract new talent to microelectronics. Here, the publicly founded DE:Sign Projects contribute through open-source tools and shared design infrastructures, while the International Summer School on Microelectronics (ISSOM) focuses on hands-on training, international exchange, and community building for students and early-career researchers.



Norbert WEHN

Professor

Department of Microelectronic Systems Design
RPTU University Kaiserslautern-Landau

e-Mail: norbert.wehn@rptu.de

Homepage: <https://eit.rptu.de/fgs/ems/start>



Norbert Wehn holds the Chair of Microelectronic System Design in the Department of Electrical Engineering and Information Technology at RPTU Kaiserslautern-Landau. He has authored or co-authored more than 500 publications in various areas of microelectronic system design and holds more than 20 patents. His research interests include VLSI architectures for mobile communications, advanced SoC architectures, DRAM controllers and interfaces, post-quantum cryptography, machine learning, IoT, and emerging design methodologies. He is currently Co-Spokesperson of the BMFTR initiative Chipdesign Germany.

References and Notes

CNN-Based Equalization for Communications: Achieving Gigabit Throughput with a Flexible FPGA Hardware Architecture, J. Ney, C. Füllner, V. Lauinger, L. Schmalen, S. Randel, N. Wehn. International Journal of Parallel Programming, June 2026.

Effect of Transistor and Interconnect Scaling on Aging in Advanced SRAM, Z. Zhang, M. Mayahinia, C. Weis, N. Wehn, M. Tahoori, S. Nassif, G. Tshagharyan, G. Harutyunyan, Y. Zorian. IEEE Transactions on Device and Materials Reliability, May 2026.

A 4.266 Gbps/pin LPDDR4X PHY with an Integrated RISC-V Subsystem Optimized for Large Bump Pitch in 12nm FinFET Technology, M. Mestice, J. Feldmann, J. Lappas, M. Esmaeilpour, C. Weis, N. Wehn. 2025 IEEE 38th International System-on-Chip Conference

AnaCraft: Duel-Play Probabilistic-Model-based Reinforcement Learning for Sample-Efficient PVT-Robust Analog Circuit Sizing Optimization, M. Ahmadzadeh, J. Lappas, N. Wehn, G. Gielen. IEEE Trans. on CAD, Volume 45, 2025

Row-Merged Polar Codes: Analysis, Design and Decoder Implementation, A. Zunker, M. Geiselhart, L. Johannsen, C. Kestel, S. ten Brink, T. Vogt, N. Wehn. IEEE Transactions on Communications, July 2024.

First demonstration of in-memory computing crossbar using multi-level Cell FeFET, T. Soliman, S. Chatterjee, N. Laleni, F. Müller, T. Kirchner, N. Wehn, T. Kämpfe, Y. Chauhan, H. Amrouch. Nature Communications, October, 2023.

Secure IoT in the Era of Quantum Computers — Where Are the Bottlenecks?, M. Schöffel, F. Lauer, C. Rheinländer, N. Wehn. Sensors, Special Issue "Lightweight Security Integrity and Confidentiality for Internet of Things (IoT)", 2022.



Microelectronic Design - It's all about Energy efficiency

Dr.-Ing. Norbert Wehn
Department of Microelectronic Systems Design
RPTU University Kaiserslautern-Landau
(e-Mail: norbert.wehn@rptu.de)

For decades, semiconductor scaling has continuously improved performance, integration density, and energy efficiency. Today, however, technology scaling is slowing down while computational demands, especially for artificial intelligence, are growing dramatically. Energy efficiency has become a key challenge in microelectronic system design. A major share of energy is no longer spent on arithmetic itself, but on memory access and data movement. In AI accelerators, transferring weights and intermediate data between memory and compute units dominate both energy consumption and execution time. We must therefore rethink the traditional separation of compute paradigms. This talk discusses promising approaches, emphasizing in-memory computing [1, 2, 3], new data formats [4, 5], and stochastic computing [6]. These concepts aim to reduce data movement, simplify arithmetic, and improve overall efficiency.

References and Notes

- [1] Sudarshan, C.; Soliman, T.; Lappas, J.; Weis, C.; Hassani Sadi, M.; Jung, M.; Guntoro, A.; and Wehn, N. “A Weighted Current Summation Based Mixed Signal DRAM-PIM Architecture for Deep Neural Network Inference.”, In: *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* 12.2 (June 2022), pp. 367–380.
- [2] Soliman, T.; Chatterjee, S.; Laleni, N.; Müller, F.; Kirchner, T.; Wehn, N.; Kämpfe, T.; Chauhan, Y. S.; and Amrouch, H. “First demonstration of inmemory computing crossbar using multi-level Cell FeFET.” en. In: *Nature Communications* 14.1 (Oct. 2023), p. 6348.
- [3] Sudarshan, C.; Hassani Sadi, M.; Steiner, L.; Weis, C.; and Wehn, N. “A Critical Assessment of DRAM-PIM Architectures - Trends, Challenges and Solutions.” en. In: *Embedded Computer Systems: Architectures, Modeling, and Simulation*. Ed. by A. Orailoglu, M. Reichenbach, and M. Jung. Cham: Springer International Publishing, 2022, pp. 362–379.
- [4] Krupp, L.; Magalhães Gomes De Souza, G.; Nassif, S. R.; and Wehn, N. *New Number Formats for FFT IP Cores in Optical OFDM Transceivers*. arXiv:2607.17835 [cs.AR]. July 2026.
- [5] Hassani Sadi, M.; Sudarshan, C.; Nassif, S. R.; and Wehn, N. “Efficient Deep Neural Network Training With a Novel 5.3-Bit Block Floating Point Data Format.” In: *IEEE Transactions on Circuits and Systems for Artificial Intelligence* 2.2 (June 2025), pp. 150–161.
- [6] Hassani Sadi, M.; Hammoud, B.; and Wehn, N. “Microscaling–Stochastic Computing Based Systolic Arrays for Energy-Efficient Deep Neural Network Inference.” In: *2026 Design, Automation & Test in Europe Conference (DATE)*. Apr. 2026, pp. 1–3.



Pengcheng Xu
Senior Researcher

Department of Electrical Engineering
Technical University of Munich

e-Mail: pengcheng.xu@tum.de

Homepage: [Xu, Pengcheng - Chair of Circuit Design](#)



Pengcheng Xu received the B.Sc. degree in Physics from Shanghai Normal University, China, in 2013, the M.Sc. degree in Integrated Circuit Engineering from Tongji University, China, in 2016, and the Ph.D. degree in Electrical Engineering from the Université catholique de Louvain, Belgium, in 2021. In 2015, he was an exchange student at Friedrich-Alexander University Erlangen-Nuremberg, Germany.

He is currently an Akademischer Rat (Senior Researcher) at the Technical University of Munich (TUM), working on analog and mixed-signal integrated circuits, power-management ICs, and energy-efficient hardware. Before joining TUM in 2023, he was a Research Associate at Fraunhofer EMFT, developing FeFET-based in-memory-computing circuits and neuromorphic accelerators. At UCLouvain, he designed and experimentally validated 2.45-GHz RF energy-harvesting systems for battery-less IoT sensors. He also has industrial IC-design experience at Huawei and Shanghai TX Electronics.

His research spans circuit and system design for autonomous and intelligent edge devices, including RF energy harvesting, wireless power transfer, integrated power management, and mixed-signal computing. At TUM, he is Principal Investigator of a Young Scientists project in DFG SPP 2253 "Nano Security" on low-power voltage regulators against power-analysis attacks in edge computing. His work has appeared in IEEE JSSC, IEEE TCAS-II, ISSCC, ESSCIRC, A-SSCC, and ISCAS, and he is an inventor of an international patent family on RF energy harvesting.

Dr. Xu is an IEEE and IEEE Solid-State Circuits Society member. He has served as Associate Editor of the Journal of Semiconductors since 2024, Chair of IEEE Young Professionals Germany (2023-2024), and a Technical Program Committee member of the ACM/IEEE Design Automation Conference (2022-2024)



Energy-Efficient Circuits and Systems for Autonomous and Intelligent IoT Sensing

Dr. Pengcheng Xu

Department of Electrical Engineering

Technical University of Munich

(e-Mail: pengcheng.xu@tum.de)

Future IoT sensor nodes must combine long-term energy autonomy with increasingly sophisticated local intelligence. This talk presents circuit- and system-level techniques that address these two requirements from complementary directions. First, RF energy harvesting and simultaneous wireless information and power transfer are considered as enabling technologies for battery-less and wirelessly powered sensing [1-4]. Design methodologies and circuit techniques are introduced for maintaining high conversion efficiency under low and strongly varying input-power conditions, including impedance-aware rectifier sizing and self-gating energy-harvesting architectures. Second, the talk explores energy-efficient edge intelligence, where computation is moved closer to the sensing front end to reduce data-transfer energy and latency. Mixed-signal neural-network accelerators and FeFET-based in-memory-computing architectures are discussed as examples of hardware approaches that exploit analog computation and local data processing [5,6]. Together, these techniques illustrate a path toward compact IoT platforms that can harvest their operating energy, process sensor data locally, and sustain intelligent operation under tight power constraints.

References and Notes:

1. M. Gonzalez, P. Xu, R. Dekimpe, M. Schramme, I. Stupia, D. Bol, "Limits of 2.45-GHz Wireless Power Transfer for Battery-less Sensors – A SWIPT Room Occupancy Tracking Use Case," IEEE Internet of Things Journal, 2023.
2. P. Xu, D. Flandre, D. Bol, "Analysis and Design of RF Energy-Harvesting Systems with Impedance-Aware Rectifier Sizing," IEEE Transactions on Circuits and Systems II: Express Briefs, 2022.
3. P. Xu, D. Flandre, D. Bol, "A Self-Gating RF Energy Harvester for Wireless Power Transfer with High-PAPR Incident Waveform," IEEE Journal of Solid-State Circuits, 2021.
4. P. Xu, D. Flandre, D. Bol, "Analysis, Modeling and Design of a 2.45-GHz RF Energy Harvester for SWIPT IoT Smart Sensors," IEEE Journal of Solid-State Circuits, 2019.
5. L. Zhang, P. Xu, D. Borggreve, F. Vanselow, R. Brederlow, "A FeFET In-Memory-Computing Core with Offset Cancellation for Mitigating Computational Errors," IEEE European Conference on Solid-State Circuits (ESSCIRC), Lisbon, Portugal, 2023.
6. P. Xu, L. Zhang, F. Pscheidl, D. Borggreve, F. Vanselow, R. Brederlow, "A Dynamic Charge-Transfer-Based Crossbar with Low Sensitivity to Parasitic Wire-Resistance," IEEE International Symposium on Circuits and Systems (ISCAS), Austin, Texas, USA, 2022.



Early-Career Networking on Chip Design 5th Oct – 7th Oct, 2026

Yushen ZHANG
Research Fellow

Chair of Electronic Design Automation
Technical University of Munich

e-Mail: yushen.zhang@tum.de

Homepage: <https://ce.cit.tum.de/en/eda/persons/yushen-zhang/>



Yushen Zhang received the Dr.-Ing. degree from the Technical University of Munich (TUM), Munich, Germany, in 2025. He received the B.Sc. and M.Sc. degrees in Computer Science (Informatics) from TUM in 2017 and 2020, respectively. He is currently pursuing a Habilitation (the highest academic qualification in the German system, representing an independent research track toward a full professorship) at the Chair of Electronic Design Automation, TUM School of Computation, Information and Technology. His current research lies at the intersection of electronic design automation, computer-aided design, microfluidics, and additive manufacturing, with a focus on addressing challenges across the microfluidic design-to-fabrication workflow. His work includes automated synthesis of multilayer 3D-printed microfluidic devices, fluid mixing and control, and design-for-manufacturing techniques for low-cost resin-based 3D printing. He has also contributed to the development of portable automated microfluidic systems and open-source technologies that aim to make lab-on-a-chip development more accessible. His research interests include computer-aided design, design automation, design synthesis, microfluidic biochips, 3D-printed devices, emerging semiconductor fabrication, and heterogeneous integration.



Anyone Can Print a Biochip: From Manual Designs to 3D-Printed Microfluidics

Dr.-Ing. Yushen Zhang
Chair of Electronic Design Automation
Technical University of Munich
(e-Mail: yushen.zhang@tum.de)

Microfluidics can turn a tiny piece of plastic into a powerful laboratory for diagnostics, chemical synthesis, and biological analysis. Yet designing these devices remains a highly specialized process, often requiring considerable expertise and painstaking manual work. At the same time, resin-based 3D printing is making the fabrication of complex microfluidic structures faster, cheaper, and more accessible. This raises an intriguing question: if almost anyone can print a microfluidic device, can we also make it possible for almost anyone to design one? In this talk, I will explore our work toward answering this question. I will present a collection of tools and algorithms that automate different stages of the microfluidic design process, from interactive and manual design to the automated synthesis of functional devices. I will also discuss how fabrication constraints of low-cost resin 3D printers can be incorporated into the design process to improve printability and device fidelity. Together, these efforts illustrate a shift from manually designing individual microfluidic devices toward a more automated approach in which sophisticated biochip designs can be created, optimized, and prepared for fabrication with substantially less specialized expertise. The broader goal is simple: to make the capabilities of microfluidics available to anyone who can design and print a biochip.

References and Notes:

1. Zhang, Y.; Li, M.; Tseng, T.-M.; Schlichtmann, U. Open-source interactive design platform for 3D-printed microfluidic devices. *Communications Engineering* 2024, 3, 71.
2. Zhang, Y.; Rašeta, D.; Tseng, T.-M.; Schlichtmann, U. 3M-DeSyn: Design synthesis for multi-layer 3D-printed microfluidics with timing and volumetric control. *Proceedings of the 30th Asia and South Pacific Design Automation Conference (ASP-DAC) 2025*, 1357–1363.
3. Zhang, Y.; Kundu, D.; Tseng, T.-M.; Roy, S.; Yamashita, S.; Schlichtmann, U. Accessible ratio-specific mixing: Single-pressure-driven multi-reagent mixer design and synthesis for 3D-printed microfluidics. *31st Asia and South Pacific Design Automation Conference (ASP-DAC) 2026*, 398–404.
4. Zhang, Y.; Liang, S.; Tseng, T.-M.; Schlichtmann, U. LiPCon: A physics-aware spatially resolved light penetration compensation method for low-cost 3D-printed microfluidics. *Proceedings of the 63rd ACM/IEEE Design Automation Conference (DAC) 2026*, 1–6.
5. Zhang, Y.; Chen, J.; Tseng, T.-M.; Schlichtmann, U. 3D-VASE: Volumetric-Aware Scalable and Efficient Multi-Layer Design Synthesis for 3D-Printed Microfluidics. *Proceedings of 32nd Asia and South Pacific Design Automation Conference (ASP-DAC) 2027*



Early-Career Networking on Chip Design 5th Oct – 7th Oct, 2026

Dr. Vaibhav Agarwal

Deputy Director

Deutsche Forschungsgemeinschaft (DFG)
German Research Foundation
DFG Office India

Contact Number: +91 9871881220

E-Mail: vaibhav.agarwal@dfg.de

Homepage: <https://www.dfg.de/india>



- | | |
|-----------------------------|--|
| October 2016 – now | <i>Deputy Director</i>
DFG Office India, New Delhi |
| October 2016 – now | <i>Chairperson</i>
Advisory Board
German Centre for Research and Innovation (DWIH New Delhi) |
| Nov 2014 – Sep 2016 | <i>Senior Scientific Officer</i>
DFG Office India, New Delhi |
| Jan 2009 – Oct 2014 | <i>Postdoctoral researcher</i>
Swedish Society for Medical Research (SSMF) Postdoctoral fellow
Lund University, Sweden |
| Jan 2009 – June 2009 | <i>Postdoctoral researcher</i>
Ernst Moritz Arndt University of Greifswald, Germany |
| Oct 2005 – Dec 2008 | <i>Doctoral studies (Ph.D.) (Dr. rer. nat) as DAAD fellow at</i>
Research Centre for Infectious Disease (ZINF), Julius Maximilian University of Würzburg; Max von Pettenkofer Institute for Hygiene and Medical Microbiology, Ludwig Maximilian University of Munich and Institute for Genetics and Functional Genomics, Ernst Moritz Arndt University of Greifswald, Germany |



Early-Career Networking on Chip Design 5th Oct – 7th Oct, 2026

Dr. Franziska Langer

*Programme Director
Director DFG Office India*

International Affairs

Contact Number: +49 (228) 885-3116

E-Mail: franziska.langer@dfg.de

Homepage: <https://www.dfg.de/india>



- | | |
|------------------------------|---|
| July 2022 – now | <i>Director International Affairs, DFG Office India, New Delhi</i>
Deutsche Forschungsgemeinschaft (DFG), Bonn |
| Nov 2020 – Oct 2021 | <i>Programme Officer Scientific Affairs</i>
<i>Life Sciences, Neurosciences</i>
Deutsche Forschungsgemeinschaft (DFG), Bonn |
| Jul 2014 – June 2022 | <i>Programme Officer International Affairs</i>
Deutsche Forschungsgemeinschaft (DFG), Bonn
International collaborations with partners in Asia |
| Jul 2015 – Jan 2016 | <i>Programme Officer Scientific Affairs</i>
<i>Life Sciences, Neurosciences</i>
Deutsche Forschungsgemeinschaft (DFG), Bonn |
| Jul 2012 – May 2014 | <i>Trainee in Science Management</i>
Deutsche Forschungsgemeinschaft (DFG), DFG Office New York |
| Jan 2008 – April 2012 | <i>Doctoral studies (Ph.D.)</i>
Eberhard Karls University Tübingen, Hertie Institute for Clinical
Brain Research, Graduate School for Cellular and Molecular Neu-
roscienc |



Dr. Nidhi Shrivastava



Dr. Nidhi Shrivastava is a Project Scientist at the Indian National Science Academy (INSA), New Delhi, with over five years of experience in scientific administration, international scientific cooperation, programme management, and science communication.

Dr Shrivastava holds a Ph.D. in Biological Sciences from CSIR–Indian Institute of Toxicology Research (CSIR-IITR), Lucknow. She also worked as a DHR Women Scientist at the School of Biotechnology, Jawaharlal Nehru University, New Delhi, where her research focused on drug repurposing strategies and protein aggregation associated with neurodegenerative diseases. She has authored/co-authored several peer-reviewed research publications in international journals, covering areas of molecular biology, protein biochemistry, enzyme characterization, biodegradation, and amyloid aggregation.

At INSA, she is associated with the International Division, where she coordinates bilateral and multilateral scientific cooperation, international workshops and meetings, fellowship and capacity-building programmes, and engagement with international science academies and organisations. Prior to joining INSA, she worked with Vigyan Prasara, contributing to science communication and scientific content development.



Early-Career Networking on Chip Design 5th Oct – 7th Oct, 2026

Debashis Mitra



Debashis Mitra is an ICMR Emeritus Scientist at BRIC-National Centre for Cell Science, Pune, India. Dr. Mitra's primary research interests have been molecular and cellular basis of HIV pathogenesis, host-virus interaction and anti-viral drug discovery. He was a Scientist at NCCS from 1998 to 2020 and DBT Distinguished Scientist from 2020 to 2025. He has served as a Director of DBT-Centre for DNA Fingerprinting and Diagnostics, Hyderabad from 2017 to 2020 and also as Interim CEO of DBT-Wellcome Trust India Alliance for a brief period in 2022-23. Dr Mitra is also currently Vice-President (International Affairs) of Indian National Science Academy.

Dr. Mitra's primary research areas of interest have been molecular and cellular basis of HIV pathogenesis, host-virus interaction and anti-viral drug discovery. His laboratory has contributed significantly in our current understanding of HIV-1 pathogenesis. His findings have not only increased our understanding about the role of viral proteins in HIV pathogenesis but have also advanced our knowledge about the modulation and function of host proteins during HIV infection. Finally, his laboratory has also identified a number of potent anti-HIV molecules, some of which are now being further studied for potential development for antiviral therapeutics. He has published close to hundred papers till date and has several US and Indian patents to his credit.

Dr. Mitra has received several honours and awards. He has been an elected Fellow of Indian National Science Academy, The Indian Academy of Sciences and The National Academy of Sciences in India. He was a Tata Innovation Fellow from 2012 to 2017 and was a JC Bose National Fellow from 2018 to 2023. He was awarded Y.T. Thathachari prestigious award for Biological Science in 2011 and OPPI Scientist of the year award for 2012. Dr Mitra brings with him more than 20 years of experience in research leadership positions and international interactions.



Dr. Brajesh Pandey



Dr. Brajesh Pandey serves as the Executive Director of the Indian National Science Academy (INSA). Prior to joining INSA, he served as an Associate Professor in the Department of Physics, School of Applied Sciences, Symbiosis Institute of Technology, Pune.

Dr. Pandey received his Ph.D. from the Indian Institute of Technology Kanpur in 2008. He has been teaching since 2009 and has developed more than 500 small demonstration experiments for classroom teaching. He has conducted several workshops for teachers to promote the use of demonstration experiments in science education.

Dr. Pandey has also served as a member of the Academic Committee of the Maharashtra State Board Physics Textbook Revision Committee and as Controller of Examinations for Vidyarthi Vigyan Manthan (VVM), conducted by Vigyan Prasar and Vigyan Bharati. He has served as an expert in Physics on the NCERT textbook writing committee for Classes XI and XII and as the key coordinator of the Question Bank Preparation Committee constituted by CBSE, New Delhi.

Dr. Pandey has published numerous research papers in peer-reviewed national and international journals. He has been honoured with the Dr. Vikram Sarabhai National Award for Popularization of Science for his contributions to science education and popularization.



Early-Career Networking on Chip Design 5th Oct – 7th Oct, 2026

Dr. Ina Strauß

*Programme Officer
Electrical Engineering and Information Technology
Division Mathematics and Engineering Sciences 2*

Contact Number: +49 228 885-2523

E-Mail: ina.strauss@dfg.de

Homepage: [Dr. Ina Strauß | DFG](#)



March 2022 – now

*Programme Officer
Electrical Engineering and Information Technology
Division Mathematics and Engineering Sciences 2
Deutsche Forschungsgemeinschaft (DFG), Bonn*

June 2020 – December 2020

*Postdoctoral Researcher
Institute of Physical Chemistry and Electrochemistry
Leibniz University Hannover*

October 2016 – June 2020

*Doctoral studies (Dr. rer. nat)
Institute of Physical Chemistry and Electrochemistry
Leibniz University Hannover
Coordinated interdisciplinary doctoral programme:
Hannover School for Nanotechnology - "Interdisciplinary Approaches for Smallest Sensors"*



Early-Career Networking on Chip Design 5th Oct – 7th Oct, 2026





INSA
Indian National
Science Academy



Deutsche
Forschungsgemeinschaft
German Research Foundation



IIT Madras
Indian Institute
of Technology Madras